ESD APPLICATION HANDBOOK

Design Engineer's Guide

nexperia

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Preface

Nexperia possesses industry-leading expertise in the manufacture, production and supply of the semiconductors components required for the operation of everyday electronic equipment. Our broad-based portfolio encompasses Small-Signal Discretes, Power Discretes and Analog & Logic ICs. These devices offer outstanding efficiency across a range of metrics including process, size, power and performance, while our industry-leading packages help to optimize the usage of energy and board space. Our extensive portfolio of products has been designed to address the varying demands of today's state-of-the-art applications. Our ongoing commitment to innovation, reliability and support has allowed us to become industry-leaders across key product segments. Drawing on our rich heritage of over 60 years of experience as the former Standard Product Divisions of Philips Semiconductors and NXP, we continue to develop and deliver vanguard solutions for the present and the future. Our successful record of innovation is the culmination of focused research and development across key markets, while manufacturing cutting-edge technologies on the most efficient semiconductor processes enables us to reliably provide world-class components for the most demanding markets.

Design Engineer's Guides by Nexperia

Nexperia's library of Design Engineer's Guides provides a technical encyclopedia to help you optimize your electronic designs. In this collection of technical and application insights 'from engineer to engineer', we share expertise and learnings that Nexperia's engineering teams have built up over many years of helping customers in a variety of sectors take their applications from initial concept, though prototyping and on into final production.

The first text in this collection, which was released in 2017 was the "MOSFET Application Handbook". This design guide focused on how MOSFETs can be used in specific applications and also on the impact of critical MOSFET parameters on the thermal performance of a switch. This was soon followed in 2018 by our "ESD Application Handbook", which focused on various circuit electrostatic discharge (ESD) protection concepts as well as on testing and simulation for modern Interfaces. This text was positively received by the engineering community, across various industries. To supplement the material covered in this handbook, Nexperia also offers on-site technical ESD seminars in which we share insights into a range of applications across automotive, mobile communication, consumer, computing and industrial markets. Ultimately, the aim of this handbook and accompanying seminars is to support the design community in its efforts to protect products

against damage caused by ESD related events. In 2019, the second edition of our "MOSFET Application Handbook" was updated to become the "MOSFET and GaN FET Application Handbook".

In 2020, to address the reliability challenges facing the automotive industry, we published our "ESD Application Handbook – Automotive Edition". In addition to covering ESD protection fundamentals, this text also showed how to protect classical in-vehicle networks as well as automotive Ethernet and other common interfaces found in modern automotive applications such as HDMI, USB and MIPI. Also in 2020, we released a dedicated "Logic Application Handbook" for application and design engineers who are developing and using electronic circuits, often within embedded systems. 2022 saw the release of our "Diode Application Handbook" – a technical dictionary on the past, present and future of semiconductor diodes. In 2024, we released our "BJT Application Handbook" intended as a 'go-to' reference for engineers interested in thermal properties, packaging, reliability, and applications relating to bipolar junction transistors.

We now invite you to explore and enjoy the revised and updated edition of our "ESD Application Handbook". This latest addition to our library of design guides demonstrates our commitment to ensuring that the information we provide is as up-to-date and relevant as possible, so that it more fully addresses the ever changing ESD protection challenge faced by engineers engaged in designing increasingly complex systems. The scope of this handbook has been broadened to cover applications in key mobile, consumer, automotive as well as industrial markets. This second edition now also includes vital new chapters on packaging and various aspects of quality, relevant updates which help to set this text apart as a unique and industry-leading design resource in the area of ESD protection.

This handbook is the culmination of collaborative efforts from its many valued contributors but the significant contribution of Mr. Burkhard Laue to its production deserves special recognition.

Olaf Vogt
Head of Product Application Engineering
Nexperia

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Chapter 1

Introduction

The countless number of applications for semiconductor-based devices like integrated circuits (IC) means everyday users of electronic equipment often assume that they must be inherently resilient and robust. However, what many people aren't aware of is that semiconductor-based devices have an Achilles heel that makes them susceptible to a natural and frequently occurring phenomenon – static electricity, or electrostatic discharge (ESD) as it is more formally referred to. It is incredible (perhaps even scary!) to think that such sophisticated devices, which nowadays can transport billions of bytes of data per second and even have the capacity to comfortably carry several amperes of current electricity, can be damaged or potentially even destroyed by this simple everyday phenomenon. Who could ever have thought, that something usually considered to be either a source of nuisance or fun (depending on your perspective after you receive a small electric shock from a metal handrail after walking across a carpet) could be the mortal enemy of electronic components?

This vulnerability of semiconductor devices like field effect transistors (FET) is due to the fact they are constructed using a thin oxide (insulating) layer that can be easily damaged or destroyed by electrostatic discharge (ESD) events. Additionally, a major factor in the evolution of semiconductors has been shrinking structure geometries and while this has allowed ever more functionality to be squeezed into smaller spaces, it comes with the caveat that complete systems, as well as individual ICs and data lines are increasingly sensitive to transient voltage pulses. It is therefore imperative to protect electronic components against ESD for several reasons:

Immediate or latent component failure

ESD events break down the thin oxide layers used to construct ICs, leading to internal short circuits. In the worst-case scenario, the component will fail immediately but even if it continues to function, it may have suffered latent internal damage, making it prone to failure at a later stage, thus reducing the life cycle of the equipment in which it is installed.

Reliability and safety concerns

ESD-damaged components can exhibit unpredictable behavior that significantly impacts their reliability. This can have serious ramifications, especially for critical applications like medical devices, aerospace, or automotive systems.

Cost Implications

Components can suffer ESD damage during manufacture, testing, assembly, board installation and equipment manufacture. Component failures reduce yield, thereby increasing production costs. The cost of repairing or replacing end equipment because a component has suffered ESD damage (often referred to as a field failure) is significantly more expensive.

Degraded product performance

Even if the component survives an ESD event, its performance may have been degraded, reducing accuracy or overall system efficiency.

Standards compliance

To ensure product quality and safety, many industries have introduced stringent ESD protection standards that equipment manufacturers must adhere to. Non-compliance can result in product recalls that result in reputational damage and possibly even legal penalties.

Internal ESD protection structures do not provide adequate protection

While ICs typically include internal structures to help protect them, these are usually only sufficient to guard against the type of ESD events that can occur during production and end-equipment manufacturing, which usually take place in relatively ESD-safe environments anyway. Internal structures are unable to protect ICs against the type of ESD events devices that can be experienced in the field. Therefore additional external ESD protection devices that can withstand extremely high pulse voltages of up to 30kV (peak) voltage, for a duration of up to 100ns, are required. Apart from transients, ESD protection devices must also be able to survive lower voltage but longer duration (~60 µs) surge events.

External ESD protection devices must respect signal integrity

Nowadays, electronic components play a crucial role in data communications, allowing the near-instantaneous flow of massive volumes of information in applications ranging from data centers to mobile phones to automobiles. The electronic components that enable these disparate use cases also require protecting against ESD events but this must not come at the expense of system functionality. For example, modern high-speed data interfaces operate with reduced voltage levels and at very high data rates (tens of Gbit/s), so to maintain signal integrity, printed circuit boards (PCB) require careful design using appropriate impedance matching to prevent unacceptable signal losses and reflections. It is imperative that external ESD protection devices protecting the transceiver interfaces on these boards do not negatively impact signal integrity, otherwise data could be lost or corrupted during transmission.

Nexperia has ESD expertise

Over the course of several decades, Nexperia has accumulated vast expertise in the design and manufacture of ESD protection devices as part of its broad portfolio of discrete, logic, and MOSFET products. Nexperia's ESD protection technologies have evolved with the trends towards miniaturization and offer the highest level of protection in the industry's smallest packages, with minimal impact on signal integrity. Readers of this handbook can harness this expertise to help them decide on the type of ESD protection that is most appropriate for their application.

This text provides information about the physical layers for selected data interfaces used in mobile, computing, and consumer applications as well as for interfaces used in automotive applications. These physical layer specifications are relevant for selecting suitable ESD protection devices, maintaining signal integrity, and choosing a suitable topology that respects the signal levels and the structure of drivers and receivers.

In Chapter 2 of this handbook, the fundamentals of ESD are reviewed, including its sources and the symptoms of ESD failures in electronic circuits.

Chapter 3 discusses principles of ESD protection and presents several different approaches that can be used to protect electronic devices against ESD and surge events including diodes, varistors and others.

In Chapter 4, the most important datasheet parameters for ESD protection devices and their relevance for ensuring properly functioning interfaces are described.

Chapter 5 considers the relevant testing standards for ESD and surge protection including IEC61000-4-2, ISO10605, IEC61000-4-4 and others. Test procedures for ensuring compliance with ISO standards for immunity to transients on voltage supply lines for automotive electronic control units (ECU) are also addressed in this chapter.

Radio frequency (RF) measurements, signal integrity and testing methods for ESD protection devices are the subject of Chapter 6 which also includes a deep dive into s-parameters, PCB de-embedding and T-checks. This chapter also considers the impact of ESD protection devices on high-speed serial interfaces, compliance testing as well as layout and routing of ESD protection devices for optimizing signal integrity.

Chapter 7 looks at the operation of and requirements for protecting some commonly used data interfaces like USB and PCIe as well as video interfaces such as HDMI and MIPI(D-PHY, M-PHY, C-PHY). It also discusses approaches for protecting industrial and automotive Ethernet network interfaces operating at various data rates from 10Mbps up to several Gbps using different cables as well as automotive applications like FPD-link, APIX and GMSL. Antenna interfaces are also discussed in the chapter, as well as requirements for RF antenna ESD protection.

Chapter 8 presents a latch-up analysis for deep-snap back devices and shows how electromagnetic interference (EMI) scanners can be used in time-domain ESD analysis.

Chapter 9 considers the whole system modeling of the signal pathway from the external connector to the protected IC, including internal and external ESD protection devices, the PCB itself and other discrete components. Using SPICE models for s-parameter analysis of how ESD devices affect signal integrity is also considered. Additionally, this chapter introduces system efficient ESD design (SEED) methodology for simulating the ESD protection devices' behavior and system chip interfaces as individual blocks as well as in combination, in order to determine if the two components are suitable for being used together to guard against ESD and surge events.

Finally, Chapter 10 focuses on Nexperia's wide range of package options for ESD protection devices. It also presents guidelines for making the right choice of product package by matching the application requirements with the technological characteristics of the package such as electrical, geometrical, robustness and ease of processing.

Chapter 2

ESD fundamentals

2.1 ESD physics

Electrostatic charges are generated by an imbalance between negative and positive charges on surfaces. These charges are often created by the so called triboelectric effect. Charge can be transferred when objects touch or slide against each other. Sliding and friction increases the area of contact where the distance between two objects is at the scale of molecular structures. This makes the generation of charge more effective, but the physical effect of charge separation is the same as for simple contact.

Work function Φ, measured in electron Volts (eV), is the minimum energy required to remove an electron from a solid material's surface. With a difference of the work function between materials, a lower energy state after contact can be achieved with a transfer of electrons. The exchange of electrons stops once the voltage potential between the contact partners has reached a certain level.

In the triboelectric series, materials are ranked according to their tendency to provide or collect electrons if they are in close contact with each other. The list below shows some examples, starting with materials having an affinity to spend or lose electrons normally and become charged with a positive polarity. Materials further down the list tend to collect electrons and become charged with a negative polarity.

Table 1: Triboelectric series

1.	Fur
2.	Glass
3.	Human skin
4.	Nylon
5.	Wool
6.	Silk
7.	Aluminum
8.	Cotton
9.	Steel
10.	Wood
11.	Amber
12.	Lead
13.	Sulfur
14.	Copper
15.	Gold
16.	Silver
17.	Polished Steel
18.	Brass
19.	Nickel
20.	Iron
21.	Platinum
22.	Polyester
23.	Celluloid
24.	Silicon
25.	Teflon (PTFE)
26.	Polyethylene

Well known ways of creating significant electrostatic voltages are rubbing amber with a cat fur, walking with a shuffling gait and rubber soles on a synthetic carpet, sitting down and standing up from a seat covered with synthetic fabric, and even opening and unwrapping plastic packaging. Surfaces of insulating materials can easily generate high voltages because charge is not spread over the entire surface. Figure 1 illustrates these principles.

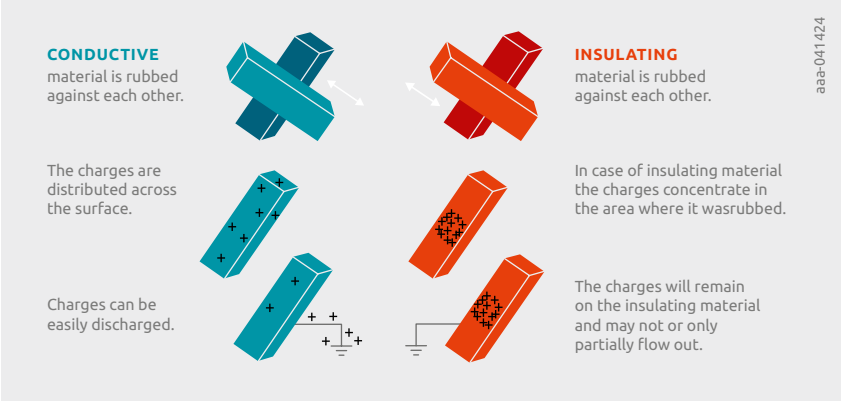


Figure 1 | Generation of electrostatic charges and influence of the material characteristics

Figure 2 shows the voltage to which a person can become charged after being in contact with the mentioned materials. When air humidity is relatively low, for example in a heated room in wintertime, electrostatic voltages can become much higher than in a damp environment.

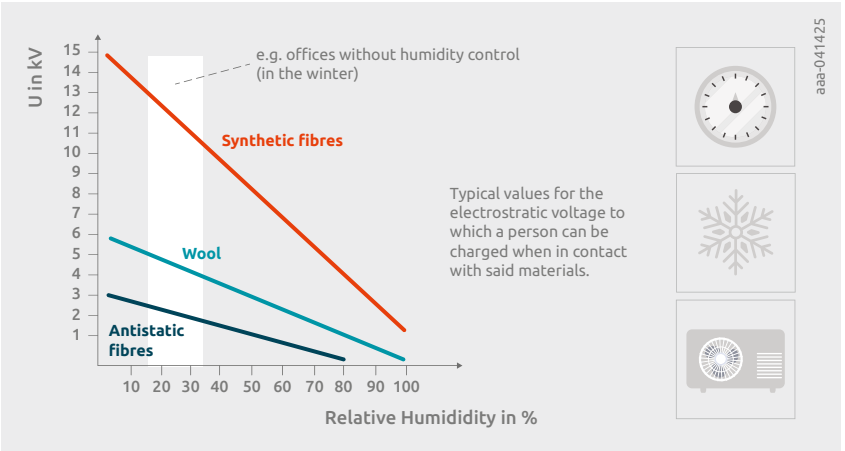


Figure 2 | Typical voltage to which a person can become charged dependent on relative humidity

After generation of a high static voltage, it is likely that a discharge will occur, during which the voltage difference is equalized in a short time. This effect is called an Electrostatic Discharge (ESD). Discharge through a human body takes nanoseconds only and peak current can be extremely high, the region of 30 A. Discharges of about 3 kV can be felt, above 5 kV the discharge can be heard, and above 8 kV a small flash can also be seen.

2.2 Symptoms of ESD failures in electronic circuits

Electronic components can be extremely sensitive with respect to ESD events. The gate oxide of small MOSFETs without integrated ESD protection can be damaged by small voltages in the region of 60 V–100 V. It is dangerous to remove such components from the conductive tape they are delivered in and perform electrical tests on a laboratory table outside an ESD Protected Area (EPA) or to not follow all the rules for safe working with ESD-sensitive devices. The floor in an EPA must be dissipative and have a high-ohmic ground termination. Also, chairs, surfaces of tables and mats must be dissipative. Persons working in an electrical protected area must wear an ESD wristband and special ESD shoes, and test this equipment daily for proper function before entering the clearly defined protected area.

With the miniaturization of structures in integrated circuits (ICs) and a decrease of supply voltages, electronic components have become more vulnerable to ESD events.

Damages that can appear can affect the following structures of a device:

- Gate oxide (MOSFET)
- Metallisation (aluminium or copper tracks inside integrated circuits)
- PN junctions (e.g. in bipolar circuits)
- Polysilicon resistors (resistor-equipped transistors, integrated circuits)

ESD damage can affect electronic devices severely, so that they no longer function. But they can also suffer pre-damage, which weakens but does not destroy them and is hard or even impossible to detect. Due to a potentially reduced lifetime, failures in the field can occur after products have been delivered to end-customers. This can damage the reputation of a company or brand and lead to excessive costs of field returns, replacement of all units delivered into a market and the need for other corrective actions.

Figure 3 and Figure 4 show some examples of damaged crystals. The failures depicted in Figure 3 can be detected by measurements if they occurred before the test. The failures shown in Figure 4 are hard to measure and can lead to reliability issues even after years of use.

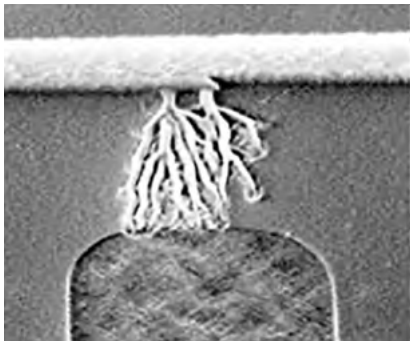
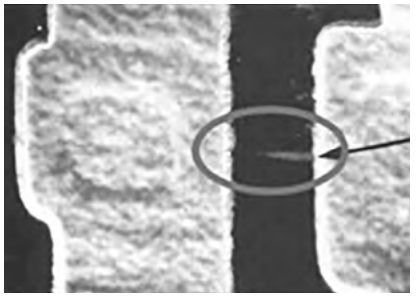


Figure 3 | Examples of destructive ESD damage



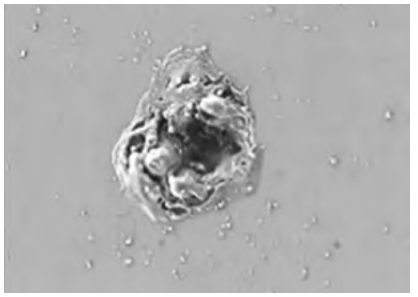


Figure 4 | Failures due to ESD damage, which are often impossible to measure

Chapter 3

Principles of ESD Protection

Several different approaches can be used to protect electronic devices against ESD and surge events.

- **Narrow gap or spark gap approach**
  A simple and inexpensive approach is to add a narrow gap between ground and the signal line. Whenever a significant ESD event occurs, an air discharge limits the high voltage pulse.
  Spark gap components operate on the same physical principle, and adding a spark gap to a signal line is a straightforward approach. The disadvantage of this kind of ESD protection is comparatively poor performance in terms of the achieved clamping voltage, which has a slow turn-on time and extremely high trigger voltage. The average dielectric air strength is about 3.3 kV/mm. This is why spark gaps are rarely used in automotive applications and are not suitable to protect higher speed interfaces.

- **Varistors**
  Varistors are often used for ESD protection. These parts are made with ceramic ZiO grain material in a mixture with other metal oxides. Varistors have a symmetrical non-linear I-V curve which shows a high resistance for lower voltages. When the varistor reaches breakdown voltage, it starts conducting. Varistors deteriorate after exposure to surge events. Older generation varistors show a weak damping of the first spike in IEC 61000-4-2 testing, however newer generation varistors are much improved. Unfortunately, the clamping voltage for the second shoulder remains significantly higher compared to silicon-based solutions. Therefore, and because of degradation concerns, varistors are not the first choice for protecting electrical interfaces.

- **Silicon-based ESD protection**
  Silicon-based ESD protection devices are the preferred choice as they show no degradation after surge events if the specified limits are adhered to. A range of topologies is available, from simple to more sophisticated, and are presented in several scenarios in this Handbook. Silicon-based ESD protection is recommended with best and lowest clamping voltage performance, as explained on the subsequent pages of this section.

3.1 Unidirectional ESD protection with a Zener diode

A simple ESD protection method and topology is a Zener diode placed between ground and signal line, as depicted in Figure 1. Surge pulses are clamped to a voltage V_{CL} according to the equation:

$$V_{CL} = V_{BR} + I_{PP} \times R_{dyn}$$

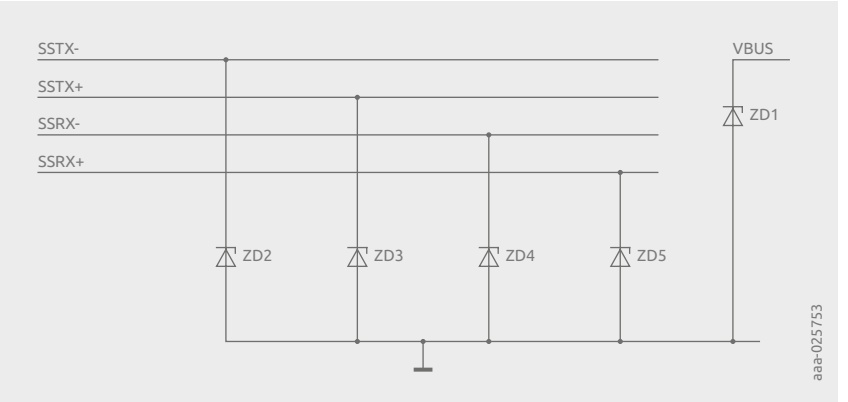


Figure 1 | ESD protection based on Zener diodes

Figure 2 shows a typical Zener diode I-V curve. The left side of the curve shows the Zener diode in the reverse bias region. The current is small if the test or operating voltage remains below the stand-off working voltage, V_{RWM}. Below this voltage, reverse leakage current is smaller than the specified I_{RM}. When the voltage increases, current increases suddenly, at which point the avalanche region begins, marked by the breakdown voltage V_{BR}. The breakdown voltage is measured in a current-driven test set-up that pushes 1 mA through the diode.

The right side of the curve shows the Zener diode in the forward bias region. The current is picking up if the voltage exceeds V_F. Negative surge pulses are clamped to low voltages ($V_F \approx -0.7$ V). The described topology forms a unidirectional protection.

A Zener diode creates a unidirectional protection for an interface, clamping at low voltages for negative surge events above V_F, as well as clamping voltage – according to the V_{CL} equation – for positive surge events.

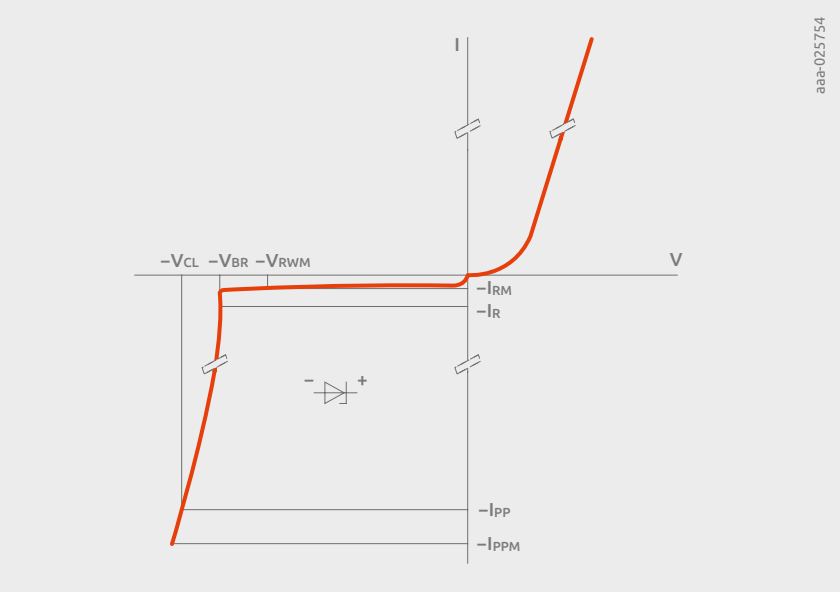
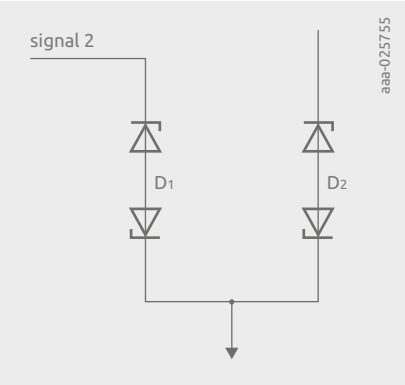


Figure 2 | I-V Curve of a Zener-diode or avalanche-type ESD protection diode

3.2 Bidirectional ESD protection with a Zener diode

If two Zener diodes with opposite directions are connected in a series, as shown in Figure 3, a bidirectional ESD device is created. If the two diodes are identical, the I-V curve is symmetrical, as shown in Figure 4.

Figure 3 | ESD protection with a bidirectional ESD protection diode



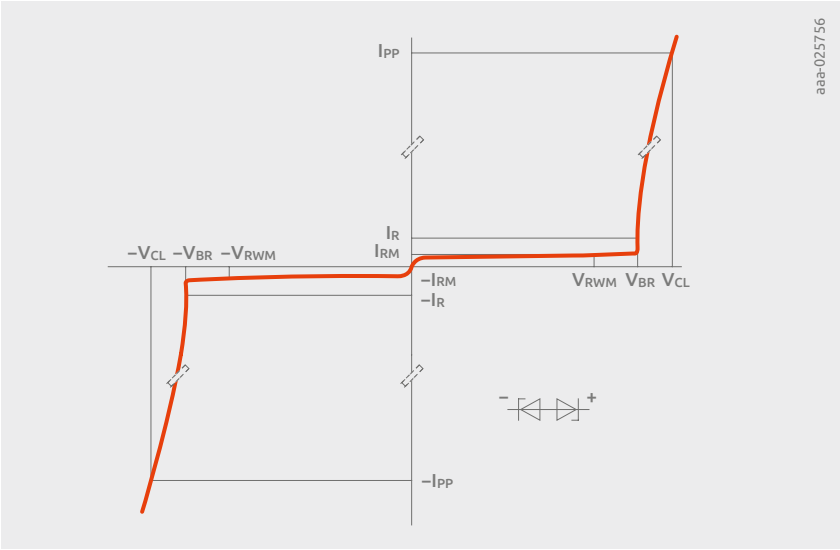


Figure 4 | I-V-Curve of a bidirectional ESD diode with simple avalanche breakdown behavior

Calculation of the clamping voltage is the same as the equation for the reverse direction of unidirectional ESD diodes:

$$V_{CL} = V_{BR} + I_{PP} \cdot R_{dyn} \quad with \quad V_{BR} = V_{BR1} + V_F$$

The V_F value is adding a portion to V_{BR} and the reverse breakdown V_{BR1} of the other diode. Bidirectional ESD protection must be applied to interfaces operating with positive and negative voltage ranges (f example, analog audio signals). Most digital interfaces that only operate with positive voltages can be protected with a unidirectional solution, although many designers make use of bidirectional ESD protection. The SoCs are exposed to much higher negative clamping voltages for negative ESD strikes. This should be avoided if possible because it can severely affect system-level robustness. Especially for automotive in-vehicle networking interfaces, bidirectional protection devices are mandatory to comply with the large voltage range allowed on the data line and to meet EMC requirements. The negative clamping behavior is not an issue, because these SoCs are designed to withstand such negative surge events and aditional circuitry, like common-mode chokes (CMCs), or ferrites are damping the amplitude additionally.

When designing low-capacitance ESD protection components it can be helpful to choose a structure with two ESD diodes in series because the parasitic capacitance is lower compared to a unidirectional device, as the well known equation below shows:

$$C_d = \frac{C_1 \cdot C_2}{C_1 + C_2}$$

Another reason for choosing bidirectional ESD diodes is that the mounting direction is not important.

3.3 Rail-to-rail topology with pn-diodes and a Zener diode

Figure 5 shows an ESD protection environment with a rail-to-rail topology:

- From each signal line, one pn-diode is connected to the upper rail, while another pn-diode is connected from the signal node to the ground rail (GND).
- A Zener diode is connected between ground and upper rail.
- Positive surge pulses push the energy through the upper diodes towards the upper rail.
- Negative surge pulses push the energy through the lower diodes towards ground.
- To improve the ESD performance, the upper rail can be connected to the supply voltage.

The Zener diode functions as a clamping device and limits the voltage of positive surge events. If the upper rail is connected to a supply line or Vbus, current can also flow into the supply where, typically, capacitors can damp incoming pulses. As a negative side effect, microcontroller circuits can show soft fails generated by the supply voltage overshoot that is created.

The rail-to-rail structure allows a very robust structure with a high capacitance of the Zener diode. The pn-diodes are comparatively small, with a small parasitic capacitance. C_d on the signal line is roughly twice the capacitance of the pn-diode, assuming that the top and ground rail works like a short circuit for RF components. This short circuit is caused by the Zener diode's high capacitance and the relatively large capacitors usually connected to the supply line. Therefore, rail-to-rail architecture is a common topology to protect high-speed multimedia interfaces having a supply line, like USB. For IVN, where there is no supply line, the topology is used to reduce the capacitance only.

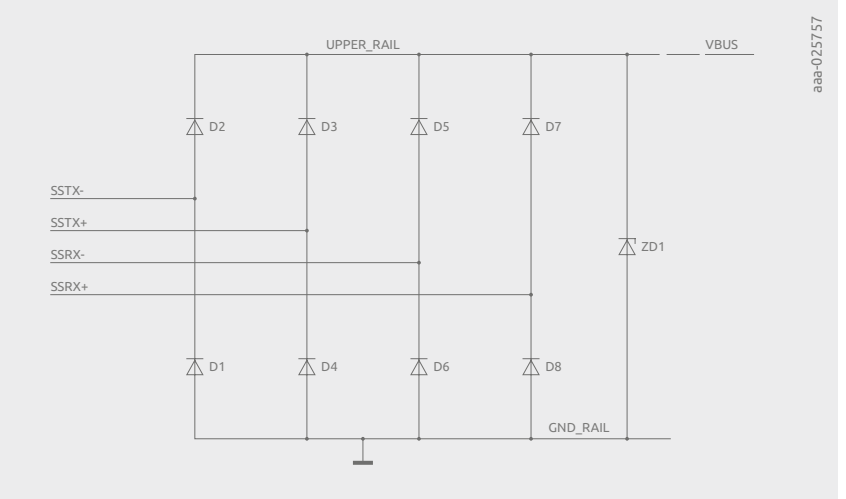


Figure 5 | ESD protection with rail-to-rail topology

3.4 Bidirectional ESD protection with open-base technology

In automotive applications, bidirectional behavior of external ESD protection devices is often desired. The classic way of achieving this is with cascaded Zener diodes. This approach is straightforward but also has some drawbacks: The clamping behavior in terms of breakdown voltage and dynamic resistance is always worse than the one of the unidirectional Zener. Furthermore, the physical implementation can exceed boundaries and increase costs significantly, as usually an additional piece of silicon and an additional bond wire are required.

Open-base technology incorporates the bidirectionality in one piece of silicon. The underlying principle is a bipolar transistor-like structure, with an unconnected base. In the event of an overvoltage, exceeding the trigger voltage, the transistor goes into avalanche. For ordinary bipolar transistors, this is a failure mode and could lead to destruction. Open-base technology based ESD protection devices are specifically designed to withstand ESD and surge pulses under these conditions. At the same time, they exhibit significantly lower parasitic capacitances than Zener diodes and an extremely low dynamic resistance. Because this is a single-chip solution, the ESD protection devices can be integrated into very small packages allowing for miniaturization and maintaining signal integrity at high frequencies.

When the transistor structure goes into avalanche, a snap-back of the voltage occurs. Depending on the physical implementation, several snap-backs can be observed. Depending on the desired application, these snap backs are tuned to behave as desired. Figure 6 shows the TLP (Transmission Line Pulse) curves of two open-base technology based ESD protections. The PESD2CANFD24V-T is designed to protect the CAN FD interface and the PESD24VF1BL is designed to protect antenna interfaces. As the CAN FD data line needs to survive 27 V DC, the snap-back is quite small. The antenna interface is not exposed to such high DC voltage, so the device can have a larger snap-back resulting in lower clamping voltages.

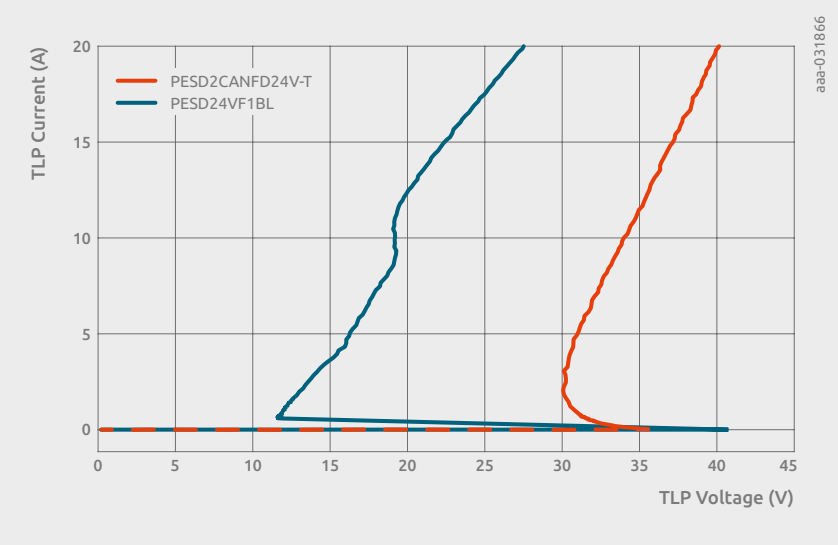


Figure 6 | TLP graph for positive polarity pulses applied to an ESD protection with open base topology, product examples PESD2CANFD24V-T and PESD24VF1BL

There is no common circuit symbol for open-base technology based ESD protection devices. Usually, two back-to-back cascaded diode symbols are used to illustrate the bidirectional behavior.

3.5 SCR topology with deep snap-back

Figure 7 shows a modification of the conventional rail-to-rail topology. Instead of a Zener diode, a silicon-controlled rectifier (SCR) is placed between the upper rail and ground. If the voltage of the upper rail exceeds a specified trigger voltage, the SCR switches into an on-state and connects the two rails. If the current through the SCR falls below a specified hold current, the SCR switches off and becomes high-ohmic again.

Note that when this protection topology is used, a supply line cannot be connected to the upper rail or to the signal inputs. In the case of a trigger event, the SCR would not return to the off-state because a DC-supply can easily provide a constant current above the hold current. The ESD protection component could be damaged, or the supply line could remain in a short-circuit condition. Therefore, in automotive applications, SCR technology is only used to protect multimedia interfaces and SerDes interfaces, when there is no risk of short-to-battery events.

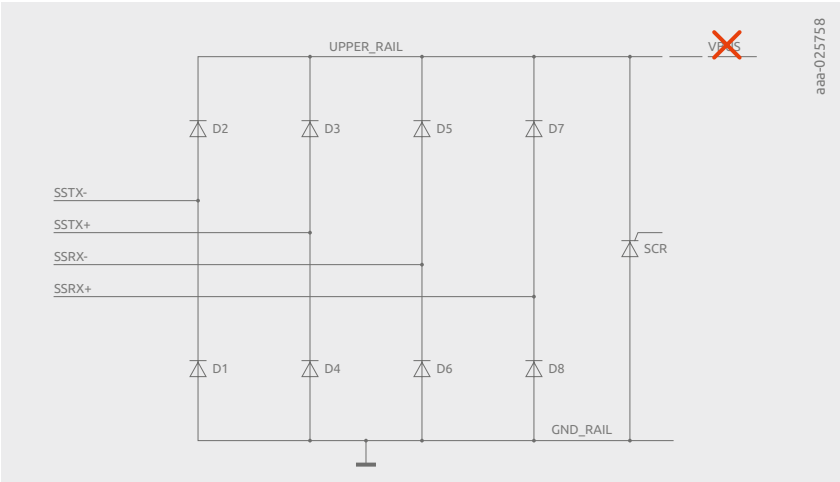


Figure 7 | Rail-to-rail ESD protection device with SCR

The advantage of the SCR-based approach is that very low clamping voltages can be achieved for surge events. The turn-on effect is often called snap-back because the voltage at the ESD protection device jumps down from a trigger voltage towards a low voltage in on-state. The snap-back voltage can be designed to drop lower than the logic high state voltage of a signal line and below V_{RWM}. Although this appears to be a conflict, in most cases it does not create a problem as Chapter 8.1 of this Handbook explains. Besides testing with a suitable I-V curve tracer, the snap back characteristic can best be evaluated with a TLP test. Figure 8 shows a TLP curve of

PESD3V3Z1BSF as an example of a TrEOS snap back device. The device triggers at about 9 V and snaps-back to 2.5 V. From there the TLP I-V-graph shows a mostly linear curve with a steepness of R_{dyn} = 0.19 Ω. Later-generation multiline protection devices offer several separate SCR protection circuits in one package. They have no rail-to-rail topology. This reduces the snap-back voltage by about 0.7 V for a unidirectional solution. After a trigger event only the signal line which was the target of a surge pulse is almost shorted to ground. The other signal lines are not affected. Figure 9 shows an equivalent circuit diagram for one channel of a unidirectional multiline protection device. Parallel to the thyristor structure, a freewheeling pn-diode conducts in case of negative surge pulses applied.

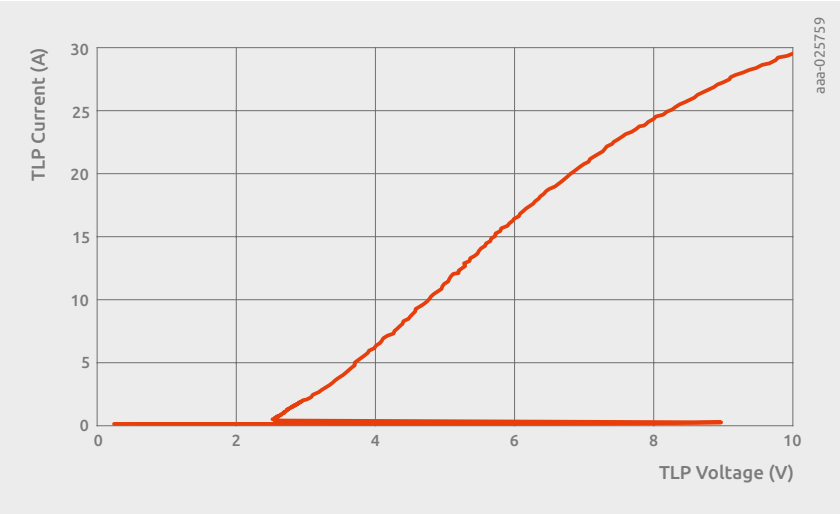


Figure 8 | TLP curve of PESD3V3Z1BSF

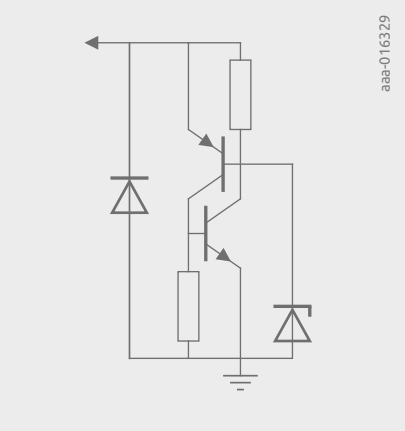


Figure 9 | Equivalent SCR circuit diagram for a unidirectional deep-snapback ESD protection device

In Figure 10, typical TLP curves are compared with each other, as described below.

- **Dark blue TLP curve:** ESD protection products based on an avalanche effect clamping topology specified for operating with a V_{RWM} between 5 V and 5.5 V. They have a breakdown voltage V_{BR} equal to or greater than 7 V.
- **Red TLP curve:** Parts that are specified for operating below or equal V_{RWM} 3.3 V have a lower breakdown voltage typically equal or greater than 5 V. Thus, clamping voltages are lower and more current of the surge event is dissipated in the protection device compared to the 5 V type.
- **Light blue TLP curve:** TLP testing can also be applied to interface pins and complete electronic products. Modern ICs often show TLP curves that start at relatively low voltages. As soon as the pulse voltage is raised, they show a steep increase of current, which is due to a low dynamic interface resistance.
  Note that many ICs can only cope with a quite low maximum TLP current. This can be I_{PP} = 5 A, for instance.
- **Black TLP curve:** This curve shows an example for a deep snap-back topology ESD diode. By adding an SCR, very low clamping voltages after turn-on of the device can be realized. Most of the surge energy is dissipated in the ESD protection and the overall system level robustness is improved. The destruction voltage marked with a cross in the light blue curve is reached for much higher currents.

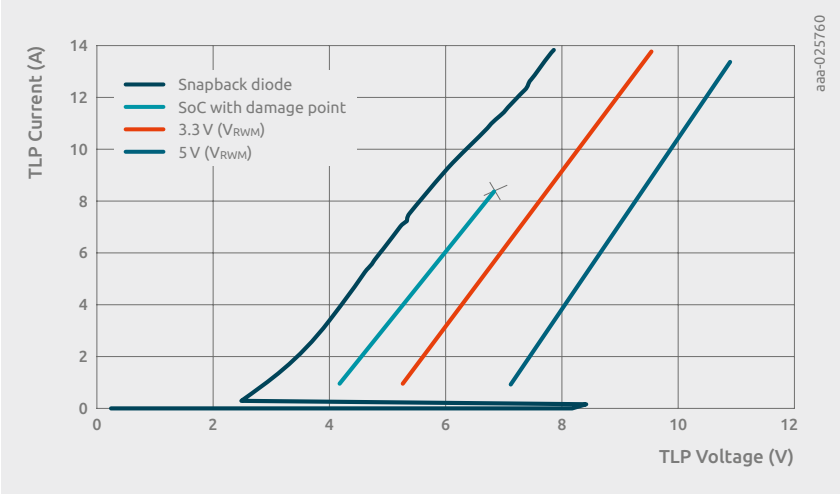


Figure 10 | TLP-Curves of three different ESD protection devices and an example curve for an interface pin of a modern SoC where the point of destruction is marked with a cross.

In conclusion, effective ESD protection requires a TLP curve for the ESD protection device that is located left of the TLP curve of the SoC. The curve must show a high steepness with no cross point to the SoC curve. In this way it can be ensured that most of the surge current flows through the protection, and only a lower current through the IC input structure. The point where the system is destroyed is shifted to higher currents. An ideal TLP curve would be perpendicular (R_{dyn} = 0 Ω), where the clamping voltage does not increase with the surge current.

With an avalanche topology, the breakdown voltage cannot be decreased any further down into the operating voltage range of the interface without causing leakages. This means that further improvement for a low clamping voltage can be driven in the direction of a perpendicular TLP curve only. However, dynamic resistance decrease has technological limits. Therefore, snap-back topology allows lowest clamping voltages and highest system protection levels for sensitive interfaces.

3.6 Common mode filter with ESD protection

Conventional digital interfaces work with single-ended signals. The logic state is defined by the voltage present on one signal line against ground level. For a logic low state, the voltage must be below a maximum allowed voltage level called VIL(max). For a high state, the signal voltage must fulfil a minimum voltage requirement defined as VIH(min). Between these two levels the logic state is not defined, so there is a 'forbidden area' through which signals may pass for transitions only. With rising clock speed and data rates, signal levels have become smaller in order to save energy and to avoid electromagnetic interference (EMI). As signal voltages decrease, single-ended signals suffer more and more from the effects of overlaid noise. It becomes more likely that the signal voltage will be temporarily located in the 'forbidden' signal area so that the logic state in a receiver cannot be recognized safely anymore. Any noise or EMI overlay on a single-ended signal can directly deteriorate the safety of the logic state recognition. Noise can be reduced with low-pass filters, but such approach limits the signal bandwidth, this means the steepness of the signal edges and the data rate possible. Single-ended interfaces often work with a high number of parallel signals as shown in Figure 11.

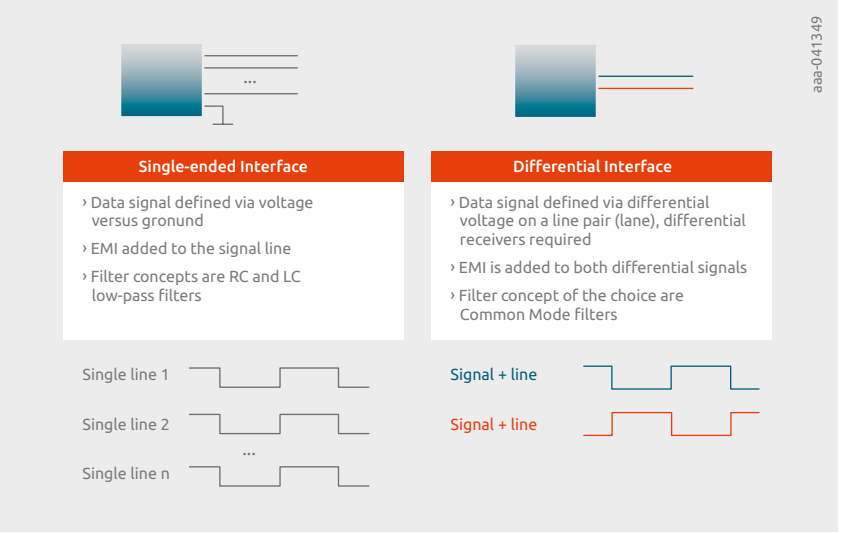


Figure 11 | Single-ended interface versus differential interface

Differential interfaces detect the logic state from the difference voltage between a positive and negative signal line. For this approach the amplitude of the signals can be comparably small. The simplest receiver for a differential signal is a comparator. The two signals of a pair are inverted to each other and each pair of signal lines is often referred to as a 'lane'. EMI or noise overlaid to a differential signal modifies both signals almost identically. Such a signal is called a common mode signal in contrast to the desired differential-mode signal which carries the logic state or data information of an interface. Differential signals are routed close to each other with an identical length in the positive and negative traces. They hardly radiate into the environment because the electrical and magnetic fields are cancelled out with some distance to the PCB traces. This is a major additional advantage of differential signals. Common mode noise can be generated from non-symmetrical driver stages and from delay or trace length differences of the differential signals on a PCB.

Common mode filters suppress the amplitude of common mode signals and allow the differential signal to pass without significant attenuation, as shown in Figure 12.

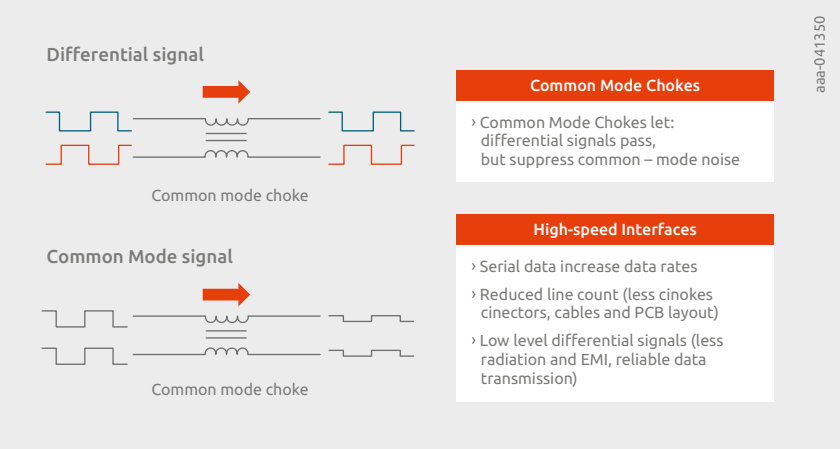


Figure 12 | How common mode filters work

Nexperia offers the combination of high performance ESD protection with a common mode filter in a single WLCSP package. For some products the combined solution of common mode filter and ESD protection can be replaced with an ESD protection-only device using the identical package and pinning as a drop-in replacement if it is found that a design does not require the filter.

This concept is shown in Figure 13. Each channel is realized with a 5-ball WLCSP structure, with input (A1, A2) and output (C1, C2) balls and a ground connection in the center (B1). Up to three channels are available in one package. The ESD protection should be placed at the side where ESD strikes are expected to enter a system. This is normally the connector on a PCB. The solution with an ESD protection and a common mode filter provides very good system-level robustness because the filter provides a small extra inductance in the path to the protected system chip. This lets the ESD protection turn on quickly and safely. Only a small amount of energy from an ESD strike can enter the SoC.

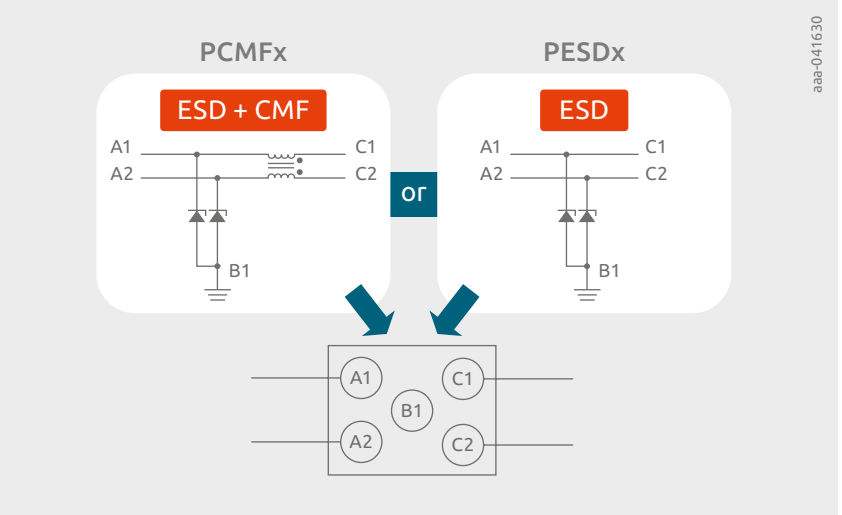


Figure 13 | Nexperia PCMFxx solution for an integrated ESD protection and common mode filter in WLCSP packages, ESD protection-only solution as alternative

Figure 14 shows the insertion loss for differential signals for the example product series PCMFxUSB3BA/C. The −3 dB bandwidth is 10 GHz. Figure 15 shows the insertion loss curve for common mode signals with a deep notch at about 4 GHz.

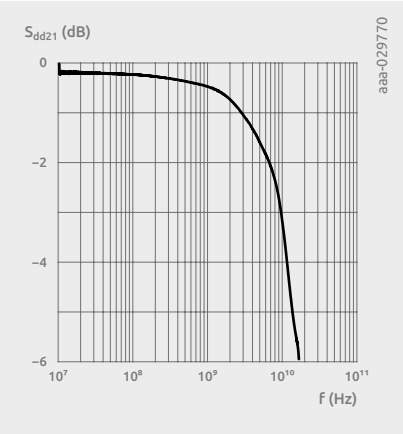


Figure 14 | Differential mode insertion loss: typical values for PCMFxUSB3BA/C

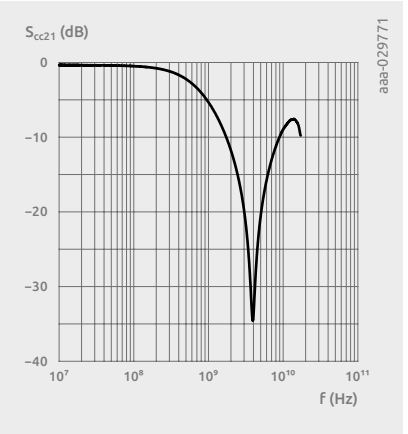


Figure 15 | Common mode insertion loss: typical values for PCMFxUSB3BA/C

Measurement tests and simulation test results for the effectiveness of different ESD protection approaches correspond very well, as shown in Figure 16. Measurement results for the residual first peak voltage at a representative super-speed SoC input are shown in solid lines. Simulated results are presented in dotted lines for an ESD protection in a wire-bonded package (DFN1006-2) as red curve, for a flat package without bond wires (DSN0603) as blue curve, and for a common mode filter in wafer-level chip scale package (WL-CSP) as green curve.

The DSN and WL-CSP packages have no bond wires. This is why they have very low peak voltages, because of their extremely low parasitic inductance of about 5 nH. Current through the protection path can increase rapidly so that low current flows into the system chip to be protected. As the green curve shows, the inductance of the common mode filter improves the result even more. The curves that are measured look very similar to simulated results concerning the peak voltages.

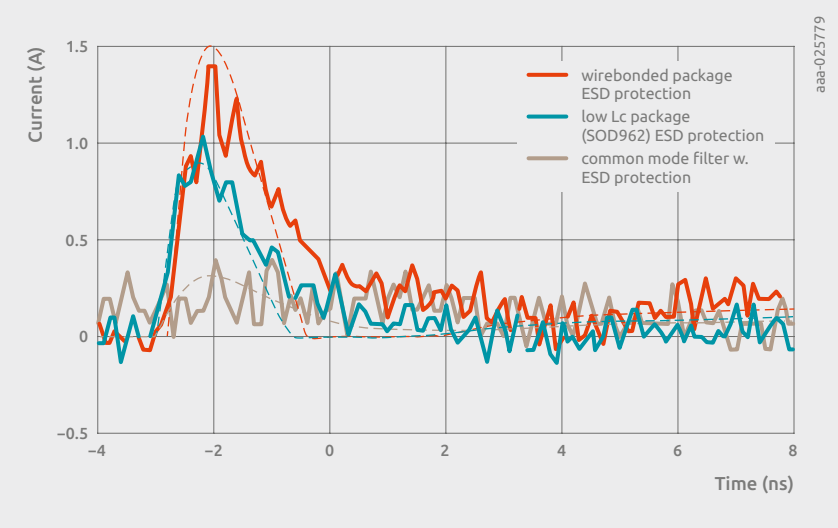


Figure 16 | Residual first peak overvoltage of an ESD strike at the SoC input

Chapter 4

Datasheet parameters of ESD protection devices

To select suitable ESD protection devices, development engineers must compare key parameters found in vendor datasheets. In this chapter, the most important key parameters and their relevance for achieving a well operating interface are described. Furthermore, signal integrity needs to be maintained to ensure that receiver circuits in digital interfaces can sample the incoming data without errors. The following sections illustrate the information presented in most datasheets for Nexperia ESD protection devices. The ESD diode PESD3V3Z1BSF is used as an example.

4.1 General description

This Section of the datasheet provides a brief description of the device. The product cluster is mentioned, as well as the ESD protection technology and topology used for the addressed ESD protection device. A short package description is included, and the main application area targeted by the ESD diode. In the example case the diode is mainly designed to protect high-speed interfaces.

4.2 Features and benefits

This Section contains a short table of key facts. For the example product, the information shown below is included:

- Bidirectional ESD protection of one line.
- Extremely low diode capacitance C_d = 0.28 pF.
- Extremely low clamping voltage to protect sensitive I/Os.
- Extremely low inductance protection path to ground.
- ESD protection up to 20 kV according to IEC 61000-4-2.
- Ultra small SMD package.
- 9.5 A maximum 8/20 µs peak pulse current.

4.3 Applications

The application Section describes the application areas in more detail.

ESD and surge protection for:

- cellular handsets and accessories
- portable electronics
- communication systems
- computers and peripherals.

4.4 Quick reference data

The most important key parameters are presented in a small table. One of these is the diode capacitance C_d which needs to be small enough to not cause deterioration in signal integrity. C_d for two test frequencies is listed with the typical value and a maximum value. The reverse standoff voltage V_{RWM} is presented. The voltage of the protected signal should not exceed V_{RWM} because while the signal stays below this voltage a very small leakage current flows through the protection diode, so that no significant ohmic load is added to the protected interface.

Table 1: Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{RWM}	reverse standoff voltage	T_{amb} = 25°C	–	–	3.3	V
C_d	diode capacitance	f = 1 MHz; V_R = 0 V; T_{amb} = 25°C	–	0.28	0.35	pF

4.5 Pinning information

Section 5 of the datasheet contains the assignment of the product pins, a simplified outline and a graphic symbol as depicted in Table 2. The exact technology is not shown here. Note that the chosen product example is a deep snap-back device from the TrEOS product family, so this product is not a simple Zener diode type. The symbol indicates that the product is a bidirectional ESD protection device only.

Table 2: Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K1	cathode	 Transparent top view **DSN0603-2** (SOD962-2)	 sym045
2	K2	cathode		

4.6 Ordering information

Section 6 in datasheets for ESD protection devices contains ordering information. As shown in Table 3, the type number and package details are included.

Table 3: Ordering information

Type Number	Package		
	Name	Description	Version
PESD3V3Z1BSF	DSN0603-2	silicon, leadless ultra small package; 2 terminals; 0.4 mm pitch; 0.6 × 0.3 × 0.3 mm body	SOD962-2

4.7 Marking

On the top of the packages a marking code can be found. For the example device selected, the PESD3V3Z1BSF, a capital letter 'U' is lasered into the upper surface of the diode. Note that marking codes are not unique for a type of electronic component from Nexperia. They are however unique to a product group such as ESD protection devices.

Table 4: Marking codes

Type Number	Marking code
PESD3V3Z1BSF	U

4.8 Limiting values

V_{RWM} is the reverse standoff voltage of a protection device. It indicates the maximum operating voltage range for which leakage current is below a specified value I_{RM}. V_{RWM} must be equal to or higher than the maximum voltage expected on a signal line.

I_{PPM} is the maximum surge current that a device can withstand if an IEC 61000-4-5 [1] pulse with an 8/20 µs timing is applied. This value gives an indication of the robustness of ESD devices if they are exposed to higher pulse energy (see Section 5.6).

For the junction temperature T_j, a maximum value is given which usually is 150°C. Beside this information, an ambient temperature range T_{amb} and storage temperature T_{stg} can be found with minimum and maximum limits.

Table 5: Limiting values

Symbol	Parameter	Conditions		Min	Max	Unit
I_{PPM}	rated peak pulse current	t_P = 8/20 µs	[1]	–	9.5	A
T_j	junction temperature			–	150	°C
T_{amb}	ambient temperature			−40	125	°C
T_{stg}	storage temperature			−65	150	°C
ESD maximum ratings						
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2; contact discharge	[2]	−20	20	kV
		IEC 61000-4-2; air discharge	[2]	−20	20	kV

[1] Non-repetitive current pulse 8/20 µs exponentially decaying waveform according to IEC61000-4-5.
[2] Device stressed with ten non-repetitive ESD pulses.

Additionally, Table 5 informs the parameter VESD as the maximum voltages that an ESD protection device can withstand, in compliance with IEC 61000-4-2 [2] (see Section 5.1). The limits in kV are given for positive and negative ESD test pulses. The datasheets give limits for contact discharge testing as well as for air discharge testing. For low-capacitance protection devices, the air discharge rating is not significantly higher than the contact discharge rating. Designers should rely on the contact discharge rating because this is much better in terms of reproducibility. The ESD rating does not indicate if a protection device will provide good protection for an interface. It has no correlation to the ESD system robustness that can be achieved. For example, if a system chip is damaged with an 8 kV ESD pulse in a system test, it does not help that an ESD diode with a +/−30 kV rating was applied. It is most important that a protection diode dissipates most of the incoming surge energy due to a low clamping voltage and a short temporal delay for taking over a significant portion of the injected surge current.

4.9 Characteristics

The Characteristics Section provides detailed information about the ESD protection device. Table 6 shows important key parameters of the component. The parameter V_{RWM} is included, as in Table 1, together with a rating for the leakage current at this voltage, I_{RM}.

V_{BR} is the breakdown voltage of a protection device. It is tested with a current-driven measurement set-up in which 1 mA test current is driven through the device under test (DUT). The voltage across the DUT is V_{BR}. This parameter should not be considered generally as the starting point of a steep area in the I-V curve like known from Zener diodes. For snap-back protection devices the value can be in an area of the I-V-curve where the device has not triggered yet. It is then just an operating point with 1 mA current through the ESD diode. The topology of the diode has to be kept in mind.

I_{RM} is the leakage current if V_{RWM} is applied to the protection device. Even the maximum value is very small and cannot hamper interfaces normally.

The diode capacitance C_d is important for the RF-performance. An ESD diode is an additional capacitance connected to a signal line. It increases rise and fall times and changes the shape of eye diagrams accordingly. This impact must be small enough so that the operation of the target interface is not hampered and that the interface related compliance tests are still passed. Test frequency in the table is 1 MHz with two different bias voltages. For 0 V the diode capacitance normally shows the maximum value. With higher bias voltage pn-junctions are wider and thus capacitance decreases. For some RF-applications the dependency of C_d on the bias voltage is an important aspect. If an antenna is protected harmonic components are created if capacitance changes with the signal voltage.

Table 6: Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{RWM}	reverse standoff voltage	T_{amb} = 25°C		–	–	3.3	V
V_{BR}	breakdown voltage	I_R = 1 mA; T_{amb} = 25°C		–	6.9	8	V
I_{RM}	reverse leakage current	V_{RWM} = 3.3 V; T_{amb} = 25°C		–	1	50	nA
C_d	diode capacitance	f = 1 MHz; V_R = 0 V; T_{amb} = 25°C		–	0.28	0.35	pF
		f = 1 MHz; V_R = 1.5 V; T_{amb} = 25°C		–	0.25	–	pF
V_{CL}	clamping voltage	I_{PP} = 4 A; T_{amb} = 25°C	[1]	–	3.7	–	V
		I_{PPM} = 9.5 A; T_{amb} = 25°C	[1]	–	5.3	–	V
R_{dyn}	dynamic resistance	4 A ≤ I_R ≤ 16 A; T_{amb} = 25°C	[2]	–	0.19	–	Ω
		−4 A ≤ I_R ≤ −16 A; T_{amb} = 25°C	[2]	–	0.19	–	Ω
f_{-3dB}	-3 dB cut-off frequency	T_{amb} = 25°C; Normalized to attenuation at 1 MHz		–	17	–	GHz

[1] Non-repetitive current pulse 8/20 µs exponential decay waveform according to IEC 61000-4-5.
[2] Non-repetitive current pulse, Transmission Line Pulse (TLP) tp = 100 ns; square pulse; pulser at 70 ns to 90 ns; ANSI / ESD STM5.5.1-2008.

With the clamping voltage parameter V_{CL} values are provided for the IEC61000-4-5 test method applying pulses with an 8 µs rising edge and decay over about 20 µs. The different surge and ESD test methods are explained in detail in Section 5.6. Two clamping voltages are listed, one for an I_{PP} of 4 A and a second voltage for the maximum current for this test condition which is I_{PPM} of 9.5 A as shown in Table 5.

R_{dyn} is the steepness of an I-V-curve, $R_{dyn} = \Delta V_{CL}/\Delta I_{CL}$. The value has been derived based on a Transmission Line Pulse (TLP) test which is an exact and fully reproducible measurement approach in which standard, rectangular pulses with a duration of 100 ns are applied to the device under test (DUT) with rising energy. Details for this test method are described in Section 5.9. A TLP-curve is not a direct I-V curve of a component or system, but a curve created from noting down TLP measurement results as pairs of clamping voltages and currents and creating a curve of V_{CL} versus I_{CL} from these. A small value for R_{dyn} indicates a good ESD protection device. If R_{dyn} is zero, the clamping voltage would be identical no matter how much current is clamped. Such ideal components cannot be found in the real world, at least not for a complete curve but in partial areas only.

Finally, the −3 dB cut-off frequency is shown in Table 6. In this case such attenuation is seen for 17 GHz for the example component PESD3V3Z1BSF.

Some of the parameters from Table 6 are shown in following diagrams, not just for one or a few specific conditions. The curves show a typical device. In Figure 1, the insertion S_{21}, the insertion loss or attenuation of a generator input signal, is depicted versus the test frequency. This curve includes the −3 dB point discussed above. More details about the scattering parameters are provided in Section 9.3.

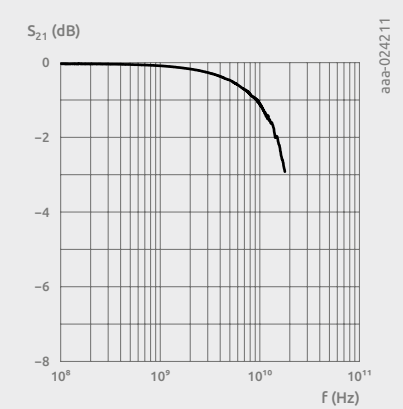


Figure 1 | Insertion loss, typical values

In Figure 2 a curve for a relative capacitance 'a' is shown for the diode parameter C_d. For a bias voltage of 0 V the maximum capacitance can be seen, so the factor a is equal one. With higher bias voltages no matter whether the polarity is positive or negative, the capacitance is decreased by a factor of about 0.85 here.

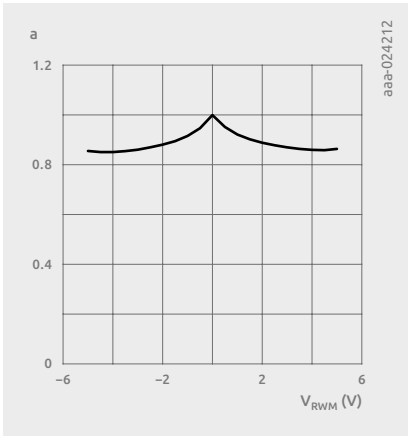


Figure 2 | Relative capacitance as a function of bias voltage, typical values

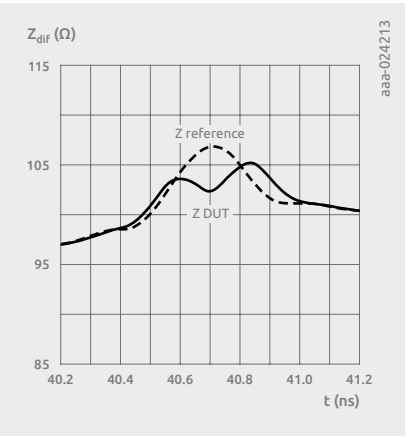


Figure 3 | Differential Time Domain (TDR) plot for rise time = 200 ps, typical values

For high-speed interfaces, it is necessary to stay within a defined impedance range for the differential impedance Z_{dif}. Figure 3 shows a time domain reflection test in which the signal applied has a rise time of 200 ps. The TDR testing approach is explained in detail in Section 6.2.

In Figure 4 and Figure 5 eye diagrams are shown for the specific target application of a 10 Gbit/s USB 3.2 signal for the chosen example of an ESD protection diode. The diodes are mounted on a small test PCB. A test PCB deteriorates the eyes already, even if no protection device is mounted. Therefore, both scenarios are included in the datasheet, the diode on the PCB in Figure 4 and the PCB without a diode shown in Figure 5.

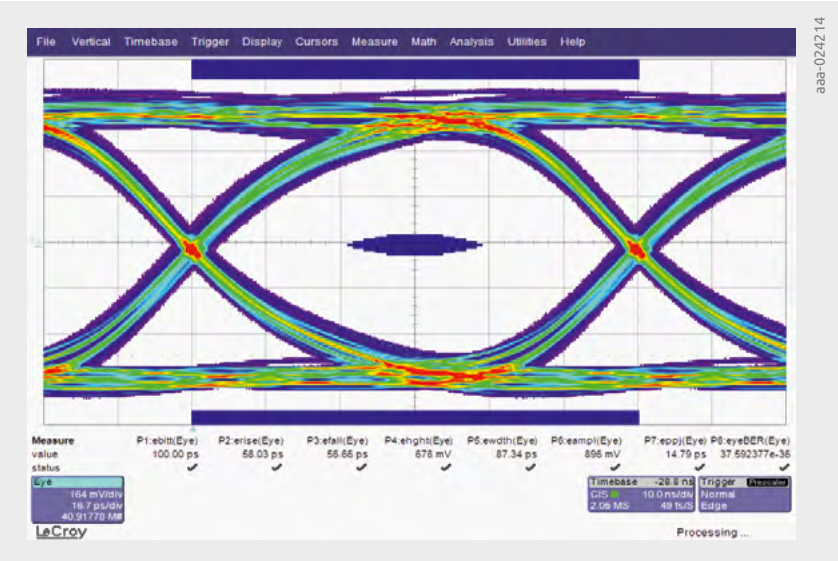


Figure 4 | USB 3.3 eye diagram, PCB with device mounted, typical values

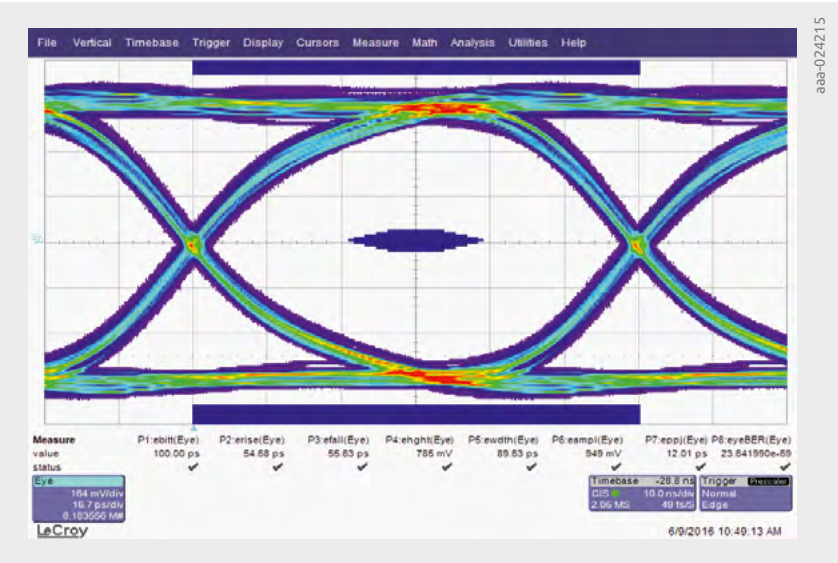


Figure 5 | USB 3.3 eye diagram, PCB without device mounted, typical values

Figure 6 and Figure 7 show TLP curves of the protection device. The curves are derived from a standard TLP test with pulses with a duration of 100 ns and 1 ns rise time. The shape of the curves is symmetrical for the positive and negative polarity. In the TLP curves it can be seen that the device snaps-back, so has a dynamic clamping behavior and not a static one like an ordinary Zener diode would show. If the voltage exceeds about 8 V, respectively −8 V, the device is turned on into a low-ohmic on-state. With the deep snap-back or turn on of the TrEOS ESD protection diode, the clamping voltage is becoming much smaller compared to the trigger voltage.

In order to judge if an ESD protection is clamping quickly it is helpful to look at the results of a VF-TLP test. Such a test is performed with pulses that have a duration of 5 ns only. Figure 8 and Figure 9 show these curves for a PESD3V3Z1BSF device. They look quite similar to the 100 ns set-up.

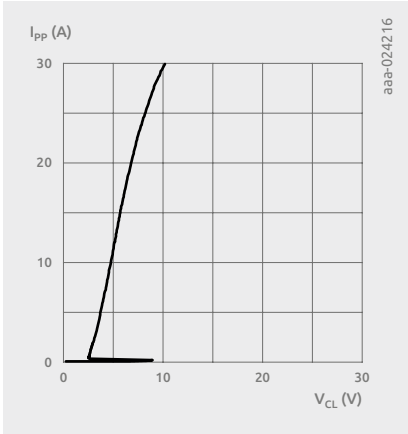


Figure 6 | Positive clamping voltage (TLP), typical values

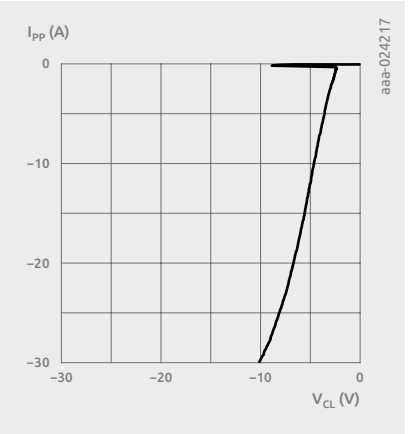


Figure 7 | Negative clamping voltages (TLP), typical values

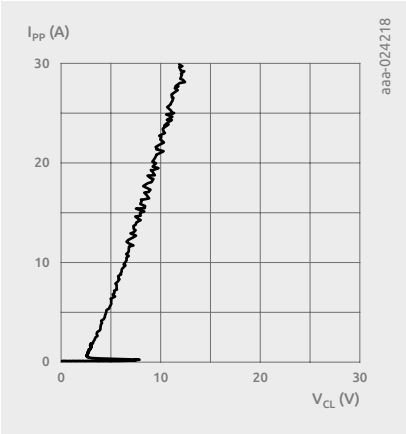


Figure 8 | Positive clamping voltages (VF-TLP), typical values

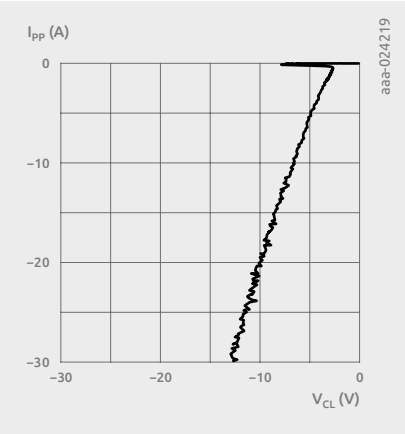


Figure 9 | Negative clamping voltages (VF-TLP), typical values

In Figure 10 and Figure 11 the peak pulse currents are depicted versus the clamping voltages for testing according to the standard IEC61000-4-5. The surge pulses rise in 8 µs and decay in about 20 µs. This method of testing is described in Section 5.6.

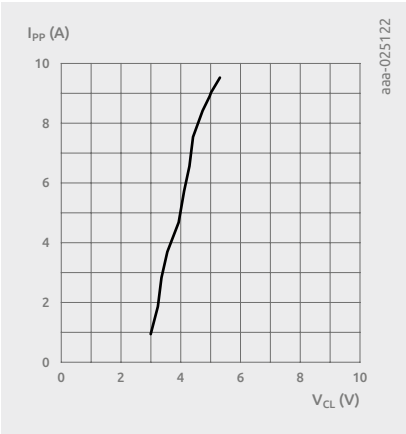


Figure 10 | Dynamic resistance with positive clamping, typical values

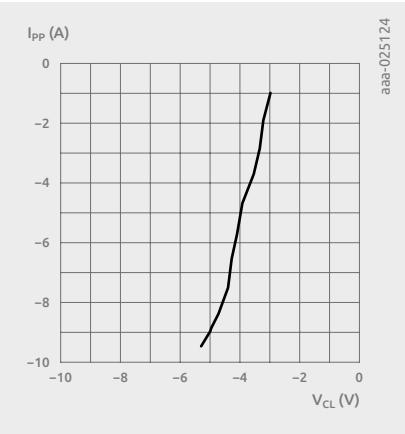


Figure 11 | Dynamic resistance with positive clamping, typical values

4.10 Application information

The application information Section of the datasheet provides basic facts about the usage and dynamic behavior of the device. For the example ESD device, which is a deep snap-back component from the Nexperia TrEOS family, the following description can be found:

The device is designed for the protection of one bidirectional data line from surge pulses and ESD damage. The device is suitable on lines where the signal polarities are both positive and negative with respect to ground. The device uses an advanced clamping structure showing a negative dynamic resistance. This snap-back behavior strongly reduces the clamping voltage to the system behind the ESD protection during an ESD event. Do not connect unlimited DC current sources to the data lines to avoid keeping the ESD protection device in snap-back state after exceeding breakdown voltage (due to an ESD pulse for instance).

Figure 12 shows an application diagram with the ESD protection device connected from a signal line to ground.

Finally, important layout and placement rules are listed. (Section 8.4 of this Handbook provides more hints and examples for a good RF and ESD layout.)

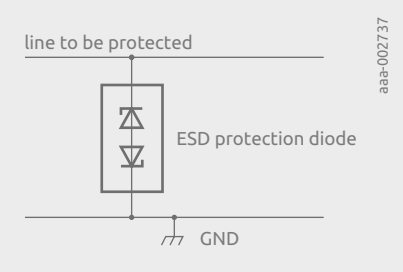


Figure 12 | Application diagram

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

1. Place the device as close to the input terminal or connector as possible.
2. Minimize the path length between the device and the protected line.
3. Keep parallel signal paths to a minimum.
4. Avoid running protected conductors in parallel with unprotected conductors.
5. Minimize all Printed Circuit Board (PCB) conductive loops including power and ground loops.
6. Minimize the length of the transient return path to ground.
7. Avoid using shared transient return paths to a common ground point.
8. Use ground planes whenever possible. For multilayer PCBs, use ground vias.

4.11 Package outline

This Section shows the dimensions and the geometrical details of the package. Tolerances of the related package are also presented.

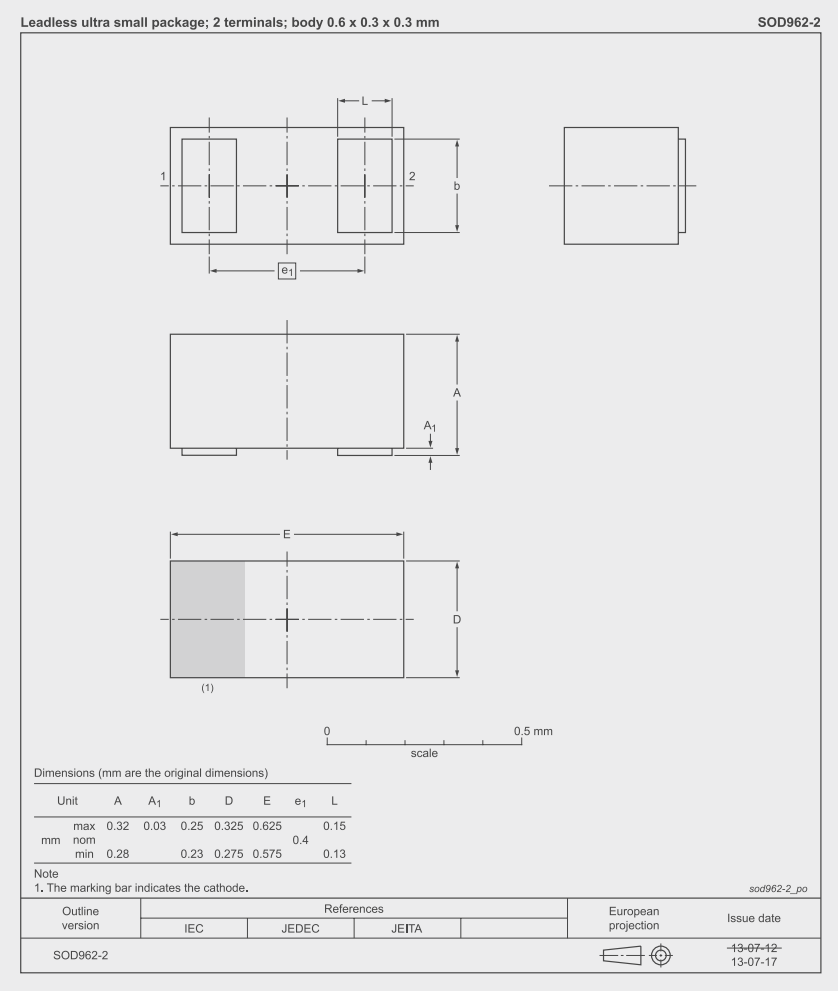


Figure 13 | Package outline DSN0603-2 (SOD962-2)

4.12 Soldering

In the datasheet Section about soldering, the dimensions of the occupied area on the PCB, the solder lands and the solder paste are presented (see Figure 14). The Nexperia website provides additional information for the soldering of small leadless packages.

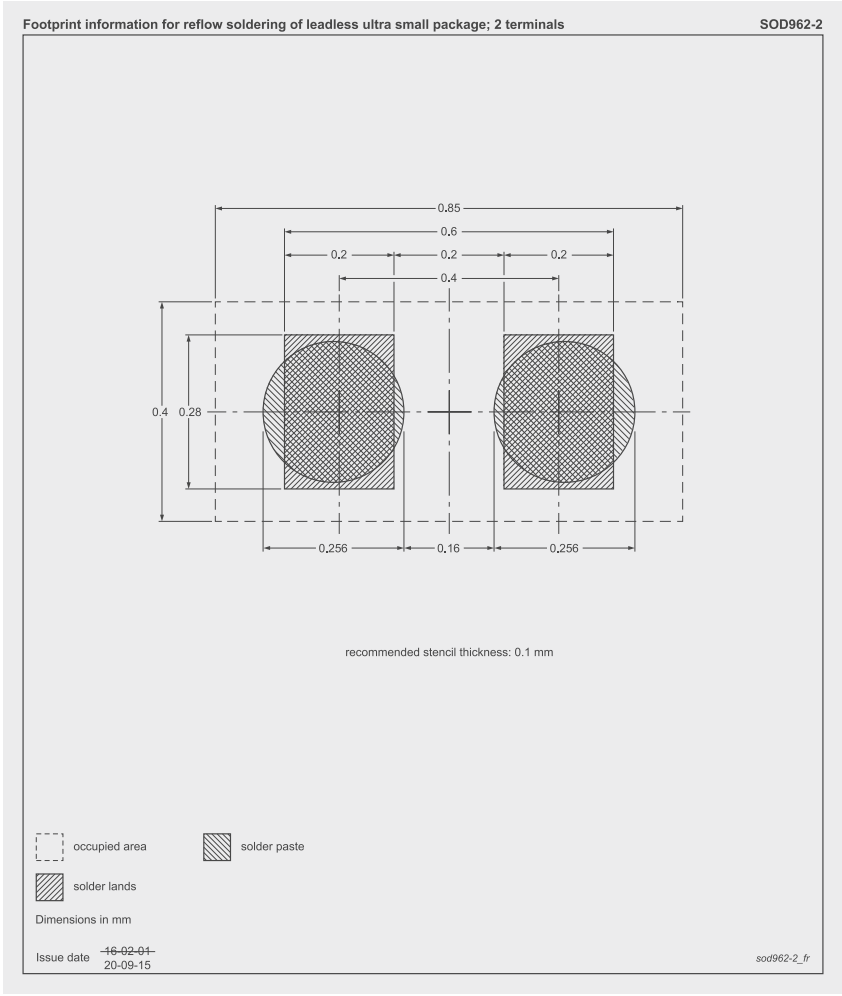


Figure 14 | Reflow soldering footprint for DSN0603-2 (SOD962-2)

References

[1] IEC 61000-4-5:2014. "Electromagnetic compatibility (EMC) — Part 4–5: Testing and measurement techniques — Surge immunity test." Geneva, CH: International Electrotechnical Commission, Jun. 2014.

[2] IEC 61000-4-2:2008. "Electromagnetic compatibility (EMC) — Part 4–2: Testing and measurement techniques — Electrostatic discharge immunity test." Geneva, CH: International Electrotechnical Commission, Dec. 2008.

Chapter 5

Testing standards for ESD and surge protection devices

5.1 ESD testing standard IEC 61000-4-2

IEC 61000-4-2 defines test methods and configuration environments for ESD robustness [1] and is commonly used to certify electronic equipment. Devices must be protected against ESD using components that can clamp and resist the high voltages defined by the respective IEC standards. The robustness of devices has to be checked and guaranteed. The tests defined in the standard are system level ESD tests in the context of EMC compliance testing.

Most electrostatic discharges occur unnoticed by users but can seriously damage gate oxides of MOSFETs used in the data path of most interfaces. In some cases, a small flash indicates that a sudden electrical discharge has occurred. The after effects are high leakage currents and malfunction of input and output circuits.

Note that when ESD protection components are mounted in a product to protect some of its sensitive parts, the behavior of these components must be tested in their final application environment. ESD pulses are generated with an ESD gun that consists of an adjustable high-voltage source with a maximum of 30 kV. A 150 pF capacitor is charged through a 50-100 MΩ resistor using a charging switch. The capacitor is discharged through a 330 Ω resistor when the discharge switch is closed. Figure 4 shows a basic ESD pulse generator schematic.

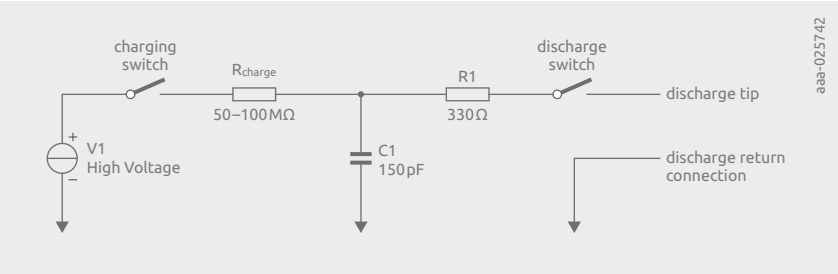


Figure 1 | ESD pulse generator according to IEC 61000-4-2

Figure 2 shows the shape of the IEC 61000-4-2 discharge current waveform of the generator shown in Figure 1. The curve behaves in the following way:

1. The pulse rises within 0.7–1 ns.
2. The first spike reaches its peak current with the peak value I_{PP}.
3. The pulse then declines within about 80 ns, including a shoulder-shape curve.

Most of the surge pulse energy is carried by the shoulder. The first spike stresses the target with high voltage and high current, but with less energy because the duration is short. Two methods are used for ESD testing: the contact measurement method and the air discharge measurement method.

Contact measurement is the recommended IEC 61000-4-2 method for ESD protection components and is set up as follows:

- The ground pin of the component is connected. The ESD gun is also connected to ground via the discharge return connection.
- The tip of the ESD gun is connected to the contact of the DUT.

In contrast to the system-level testing described in IEC 61000-4-2, the test procedure of ESD protection devices does not employ resistors (2 × 470 kΩ) in the return path. The contact discharge connection allows good reproducibility of test results. Further details of the test procedure can be found in [2].

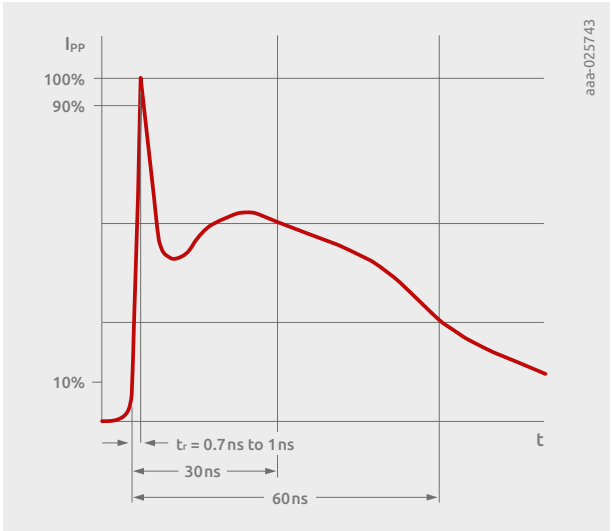


Figure 2 | IEC 61000-4-2 waveform

Table 1 lists current values for predefined IEC 61000-4-2 levels, i.e. ESD levels 1 to 4, for respective peak currents, 30 ns and 60 ns.

Table 1: ESD test waveform parameters

ESD level	voltage	first peak current, +/– 10%	Current (+/– 30%) at 30 ns	Current (+/– 30%) at 60 ns
1	2 kV	7.5	4	2
2	4 kV	15	8	4
3	6 kV	22.5	12	6
4	8 kV	30	16	8

Table 2 shows the definition of IEC 61000-4-2 ESD levels with the related minimum discharge voltages for contact discharge testing.

Table 2: ESD levels as defined in IEC 61000-4-2

ESD level	contact discharge	air discharge
1	2 kV	2 kV
2	4 kV	4 kV
3	6 kV	8 kV
4	8 kV	15 kV

For air discharge, the tip of the ESD gun is moved slowly towards the target until a flash strikes over. The results depend very much on the air humidity, the speed with which the distance between target and gun decreases, and the shape of the electrodes. Generally, this test shows low reproducibility. Often, corona discharge can be noticed without a flash if one of the two electrodes has a sharp end. In such a case, the stress on the ESD device is very low and does not lead to usable results. For the gun side, a tip with a round end is defined for air discharge, whereas the tip for contact discharge has a sharp end. The air discharge waveform has a less steep rising edge, and the surge pulse peak values are lower. Therefore, air discharge robustness is higher than, or equal to, contact discharge.

Note that technical documents must be regarded with skepticism if air discharge ratings are presented with much higher values than for contact discharge. Often, a factor of roughly 2, like the ESD level 4 definition in Table 2, is presented. Note that the voltage levels do not imply each other but are just categorizations for practical usage. Moreover, the levels defined in [1] refer to system-level testing rather than device level. It is a proven fact that for low-capacity ESD protection devices the air discharge robustness is a few kV higher or the same compared to contact discharge robustness. For this reason, air discharge testing is discouraged, not recommended, because it is much more difficult to perform correctly, and if performed correctly provides exactly the same results as contact testing [3].

Human Machine Model (HMM) testing uses the same waveform as defined for ESD guns in standard and supports 50 Ω terminated testing of ESD protection products and interfaces. The defined termination guarantees good reproducibility of test results as known from TLP tests (see Section 5.11).

5.2 Reproducibility aspects of IEC61000-4-2 testing

Figure 6 shows that the ESD gun waveform is not fully reproducible. Here, a NoiseKen gun[1] is shooting in repeat mode at a target while a high-frequency current probe[2] is measuring the current waveform. The second peak, which is located on the shoulder behind the first peak, is stable and is well within the IEC 61000-4-2 specification. However, the voltage of the first peak shows a significant variation from +25% to −35%. If target systems are sensitive to the first peak of an ESD event, test results can show a big spread, which can lead to wrong decisions being taken in the selection process of protection devices. Guns of other manufacturers show similar behavior.

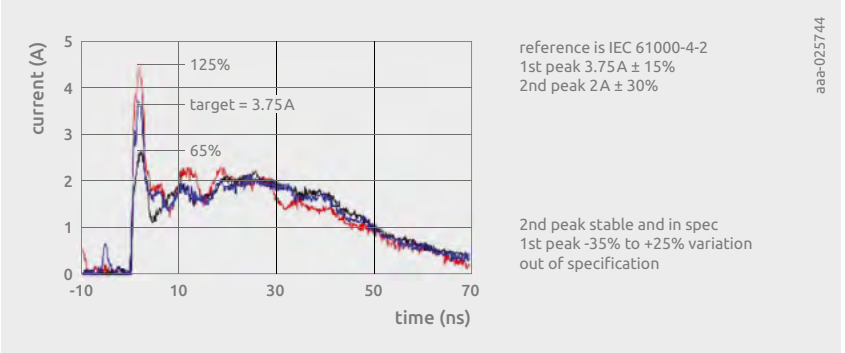


Figure 3 | IEC 61000-4-2 waveforms with NoiseKen ESS2000AX gun

Note that the grounding condition has a major impact on the voltage level of the first peak as well. If there is no proper ground close to the DUT, a small residual capacitance to ground occurs. If this is the case, the first peak loses its height and can mostly disappear. Figure 4 shows the current waveforms of two ESD gun[3] types with and without proper grounding. In set-ups without proper grounding, test results are unreliable.

1 ESS2000AX
2 F-65 current probe 1 MHz–1 GHz from Fischer Custom Communications
3 A SESD 30.000 from Schlöder and a ESS2000AX from NoiseKen

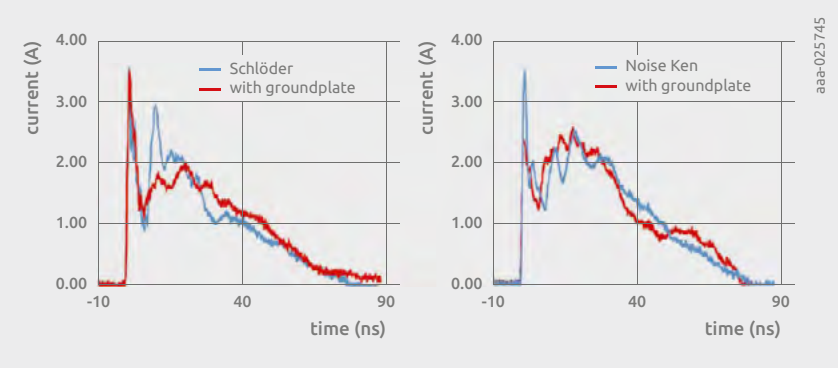


Figure 4 | Waveform comparison for ESD gun with and without proper grounding

Another risk in ESD gun testing arises when the gun is not safely connected to the DUT for contact discharge. Figure 5 shows the circuit of an ESD gun with a parasitic tip capacitance c_T of roughly 40 pF, which is significant compared to the nominal 150 pF of the ESD gun.

When a triggered gun misses the target, or when the charge moves across the switch S2, the c_T charge can discharge into the DUT with almost no series impedance. This is why the first peak of such a so called 'stray pulse' can exceed the regular pulse by a factor of 2, as illustrated by the red curve in Figure 5.

In conclusion, if a system is tested that shows an ESD sensitivity on the first peak, unsafe ESD gun connection can lead to damage at a comparatively low testing voltage, wrong test results and incorrect ESD device selection. A proper test set-up is essential to ensure reproducibility of ESD testing. More details about system level ESD testing of high-speed interface boards can be found in [2] and [3].

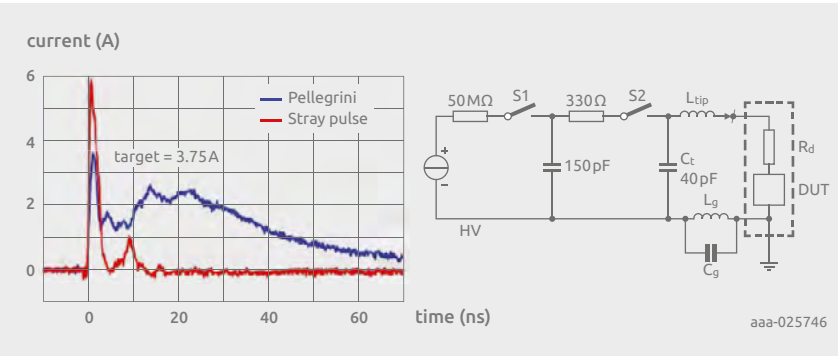


Figure 5 | Stray pulses after the target was missed

5.3 ESD testing according to the Human Body Model

The Human Body Model (HBM) standard ANSI/ESDA/JEDEC JS-001-2012 was developed to simulate the discharge of a human body to a grounded electrical device. HBM is the standard testing method to check the ESD robustness of electronic components such as integrated circuits (ICs) with respect to their input and output pins. HBM ratings are also provided for the gate oxide robustness of MOSFETs. For ICs, a 2 kV rating is an approximate standard that the semiconductor industry tries to fulfill for their products to allow a safe handling in the board production process. A simplified equivalent circuit for an HBM surge generator is shown in Figure 6. Like an ESD generator according to IEC 61000-4-2, a capacitor is charged from a high-voltage source. The capacitance is only 100 pF compared to 150 pF for IEC 61000-4-2. The discharge resistor is significantly larger –1.5 kΩ versus 330 Ω.

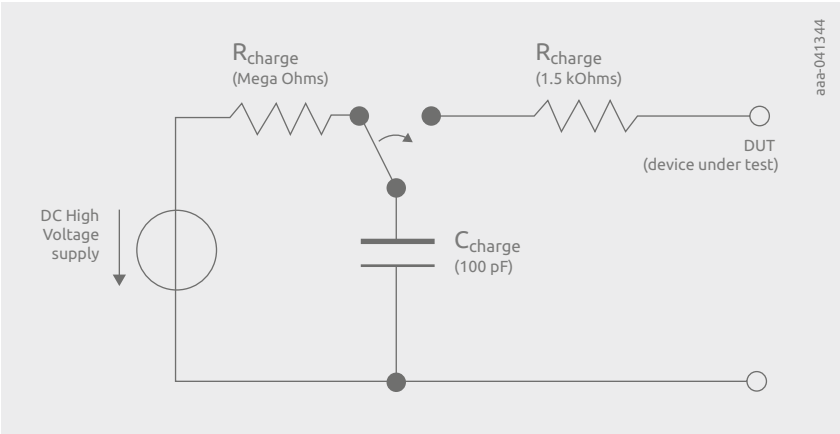


Figure 6 | Equivalent circuit for an HBM test generator

The waveform for an HBM test pulse is shown in Figure 7. An HBM pulse has a less steep rise time of about 10 ns. There is no significant first overshoot (see Section 5.1, Figure 2) and the pulse energy is smaller compared to IEC 61000-4-2 because of the smaller discharge capacitor and the higher value of the discharge series resistor. The same is true of the peak surge current, which is smaller by a factor of about 5 for the same surge voltage.

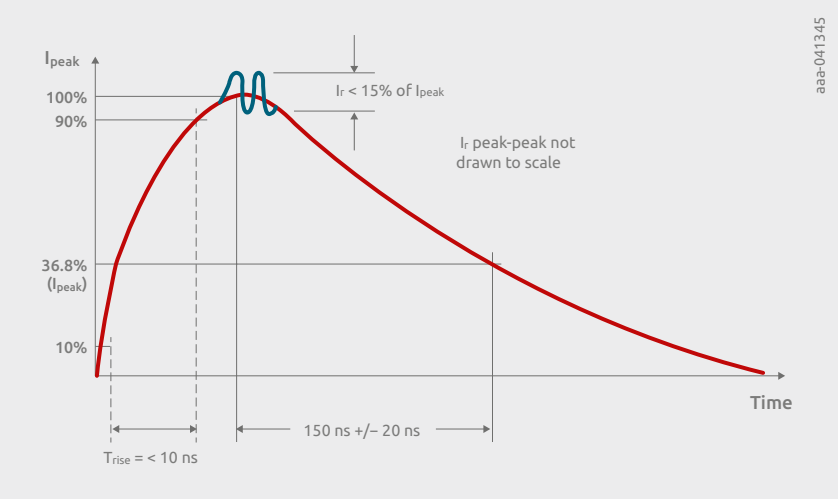


Figure 7 | HBM waveform according JEDEC JS-001-2012

5.4 ESD testing standard ISO 10605

Beside the IEC 61000-4-2 ESD testing standard, ISO 10605 is the common ESD testing standard in automotive applications. It is partially based on IEC 61000-4-2 and describes various procedures to capture ESD during assembly of the car, during maintenance and from the passenger. For the rating of ESD protection and transient voltage suppressor (TVS) devices, the waveform is of interest.

The underlying discharge network is similar to that for IEC 61000-4-2, as shown in Figure 1, with capacitance C_1 of 150 pF or 330 pF and resistances R_1 of 330 Ω and 2000 Ω. For the rating of protection device, the more severe pulse with R_1 = 330 Ω is common and both capacitor values are tested. The variant with 330 pF is more severe because of the higher pulse energy.

In contrast to IEC 61000-4-2, ISO10605 requires the ESD generator to be grounded at the car battery instead of the table. As for device tests, only contact discharge is evaluated and there is no powered case, the test setup and procedure is equal to IEC 61000-4-2 besides the used ESD generator.

5.5 EFT testing standard IEC 61000-4-4

The IEC 61000-4-4 [4] testing standard is a repetitive fast transient test which uses bursts of several short pulses. The bursts are repeated with a defined repetition rate.

Similar to IEC 61000-4-2, predefined test levels are defined as shown in Table 3.

Table 3: IEC 61000-4-4 test levels

Open circuit test voltage (+/–10%) and repetition rate of the pulses (+/–20%)				
Level	On power supply port, PE (Protective Earth)		On I/O (Input/Output) signal, data and control ports	
	Voltage peak kV	Repetition rate kHz	Voltage peak kV	Repetition rate kHz
1	0.5	5	0.25	5
2	1	5	0.5	5
3	2	5	1	5
4	4	2.5	2	5

The burst pulses have a duration of about 50 ns measured at 50% voltage levels between the rising and falling edge. Figure 8 shows the detailed definition of a single pulse. The pulses have an exponential shape of both transients and are referred to in the standard as double exponential pulses. The waveform is defined for a 50 Ω termination to ground. The duration of the pulses is 200 µs for a pulse frequency within a burst of 5 kHz, or 400 µs if 2.5 kHz is applied.

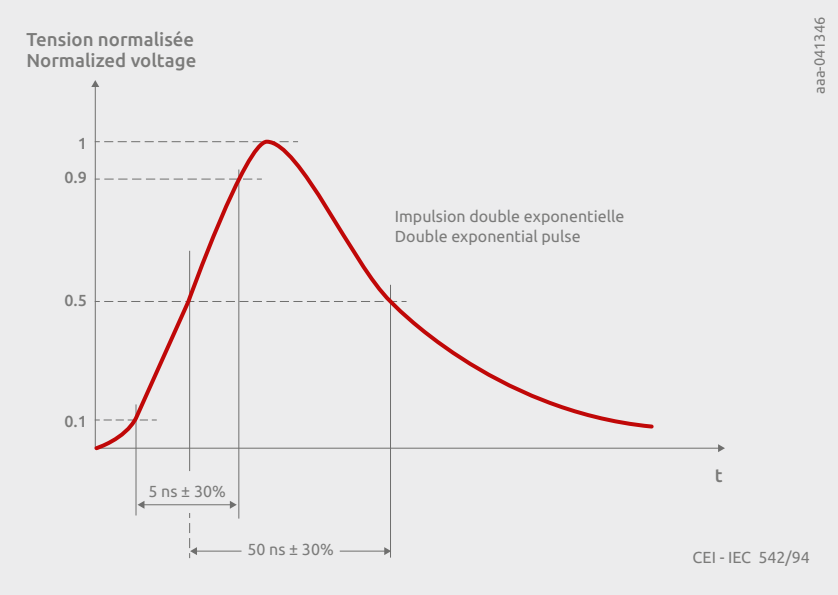


Figure 8 | Shape of a single pulse into a 50 Ω load according IEC61000-4-4

Figure 9 shows two bursts with the length of 15 ms for a burst and 300 ms as the overall time for a burst and an area without pulses before the next burst comes.

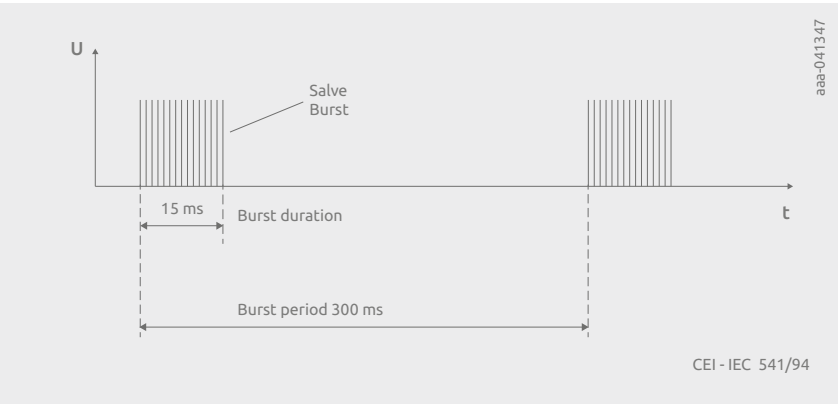


Figure 9 | General graph of a fast transient/burst

5.6 Surge testing standard IEC 61000-4-5 (8/20 µs)

Testing according to IEC 61000-4-5 [5] uses much wider test pulses than the ESD testing according to IEC 61000-4-2 [1] discussed in previous sections. The energy of surge pulses, as defined in [5], is much higher. Consequently, an ESD protection part has to dissipate more heat. The IEC 61000-4-5 standard approach simulates surge events, for instance in scenarios like power supply voltage overshoots created by load changes or overshoots caused by the plug-in procedure of chargers.

Table 4 lists key waveform data of IEC 61000-4-5 surge pulses. For the short-circuit condition of the surge generator (see Figure 9), 8 µs rise time and 20 µs fall time to 50% voltage level are defined and this is known as the 8/20 µs surge test.

Table 5 lists the relation between selected values of the peak voltage for the open circuit condition (see Figure 10) and the peak current for the short circuit case.

Output impedance of a surge generator is 2 Ω.

Table 4: Surge pulse waveform parameters

operating mode	Front time in µs	time down to 50% value in µs
open-circuit voltage	1.2 +/– 30%	50 +/– 20%
short-circuit current	8 +/– 20%	20 +/– 20%

Table 5: Open-circuit peak voltage and related peak current for the short-circuit

open circuit peak voltage +/– 10%	short-circuit peak current +/– 10%
0.5 kV	0.25 kA
1.0 kV	0.50 kA
2.0 kV	1.00 kA
4.0 kV	2.00 kA

Figure 10 shows the waveform for the short circuit condition, whereas Figure 11 depicts the surge pulse waveform for the open circuit scenario.

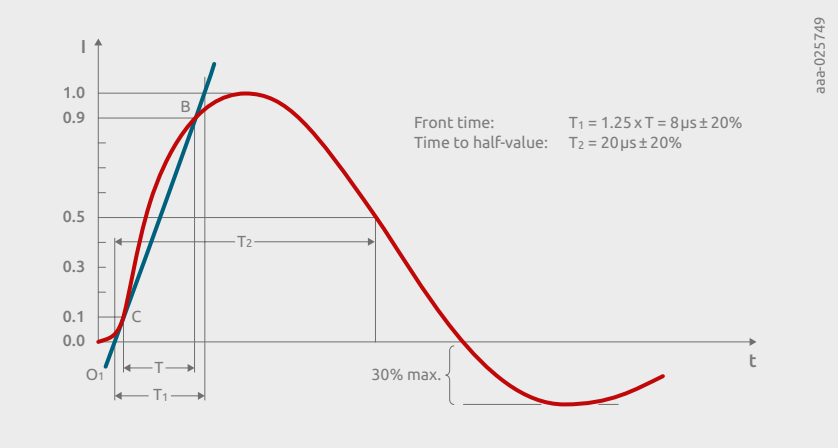


Figure 10 | IEC 61000-4-5 waveform for a short circuit condition

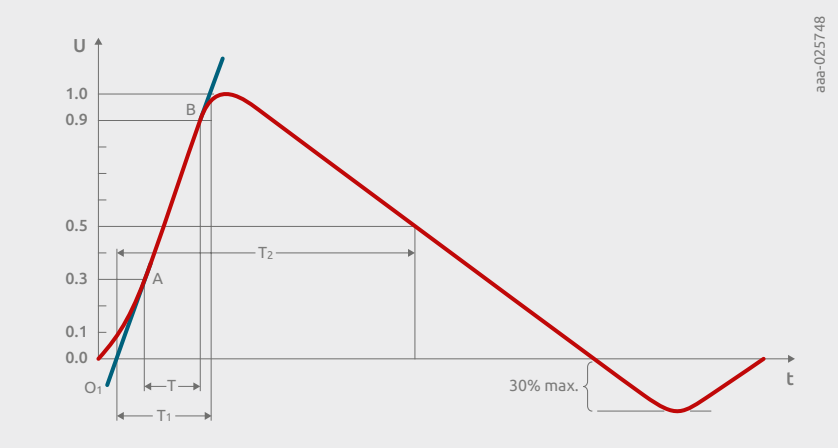


Figure 11 | IEC 61000-4-5 waveform for an open circuit condition

IEC 61000-4-5 test results deliver important datasheet parameters for ESD and surge protection devices:

- Maximum surge current I_{PPM}
- Peak power P_{PP}
- Clamping voltage V_{CL}
- Dynamic resistance R_{dyn} derived from the steepness of V_{CL} versus I_{PP} curves

5.7 Surge testing standard IEC 61643-321/-311 (10/1000 µs pulses)

Tests according to IEC 61643-321 [6] include pulses with a width much greater than defined in IEC 61000-4-5. For protection devices likely to be used in supply lines or very slow data lines, test pulses with the current waveform depicted in Figure12 are used. The rise time t1 is 10 µs and after the time t2 the pulse current has decreased to 50% of the peak level. The time t2 is 1000 µs nominal. The output resistance of pulse generators is dependent on the chosen output current range and can vary from 220 Ω down to 10 Ω.

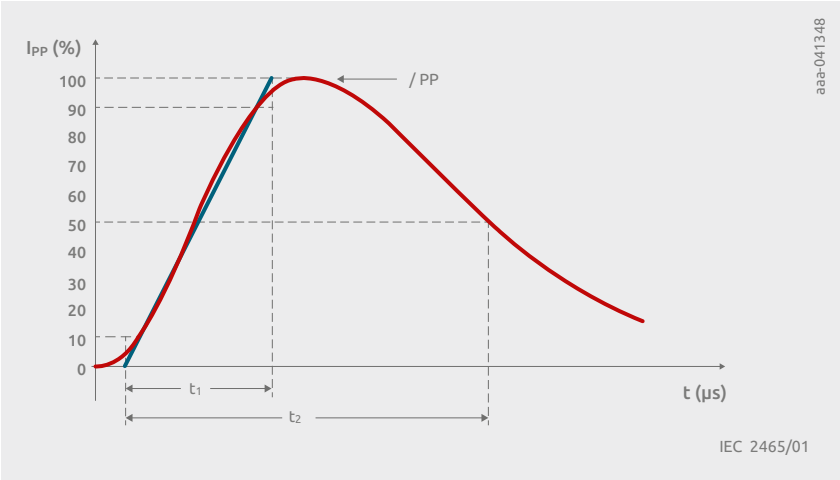


Figure 12 | IEC 61643-321 waveform for short circuit condition

5.8 Automotive transients ISO7637-2, ISO16750-2 and ISO21780

The standards ISO7637-2 [7], ISO16750-2 [8] and ISO21780 [9] specify test procedures for compliance immunity to transients on supply lines for automotive ECUs for 12 V, 24 V and 48 V board nets. As the pulses described here are only considered on the supply line and not directly on data lines, large TVS diodes that are used to protect the supply line in automotive are often required to comply system level requirements. For data interfaces, and hence for ESD protection devices on data lines, there is a risk of having a double fault condition. . This is e.g. when having a short to battery line combined with transient e.g. load dump. To cover this risk, those standards add some additional requirements for theESD protection.

- The ISO7637-2 is defining several test pulses for 12 V and 24 V battery voltage. The pulses 5a and 5b have been shifted to ISO16750-2 under the name of load dump.
- The ISO16750-2 describes the effects of electrical loads in a vehicle and how to test the DUT for compatibility. This includes various operational conditions that are not of relevance for TVS or ESD protection devices. Here, the effect of resistive behavior from the load and the resulting parasitic of the wiring harness and jumpstart condition are covered.
- The ISO21780 was recently introduced and it is defining test pulses for vehicles with 48 V battery voltage.

5.8.1 ISO7637-2 Pulse 1: Disconnecting an inductive load

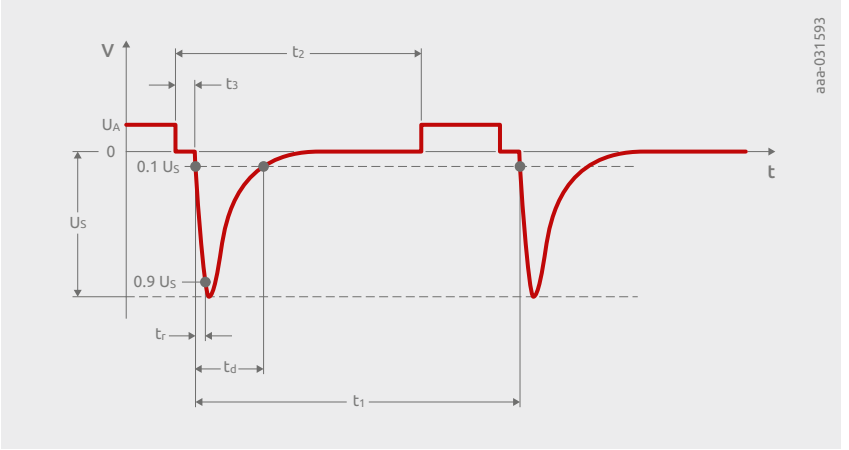


Figure 13 | Waveform of Pulse 1, disconnecting an inductive load

Pulse 1, shown in Figure 13, is representing a negative transient seen by a load parallel to an inductive load in the event of a disconnection of the power supply. The defined parameter range is very large and often corner configurations are tested to assess worst case configurations. Table 6 provides the parameter ranges and typical configurations these parameters are different for 12 V and 24 V boardnet. Ri represents the source resistance.

Table 6: Parameter ranges for Pulse 1 shown Figure 13

Boad net	U_A (V)	U_S (V)	R_i (Ω)	t_d (ms)	t_r (µs)	t_1	t_2	t_3 (µs)
12 V	13.5 ± 0.5	−75 to −150	10	2	0.5 to 1	≥ 0.5	200	< 100
24 V	27.0 ± 0.5	−300 to −600	50	1	1.5 to 3			

5.8.2 ISO7637-2 Pulse 2a: Interruption of power supply

Pulse 2a, shown in Figure 14, represents the parasitic inductance of the wiring harness. These inductance forces a positive voltage peak into the supply line of the DUT when it draws current, and the voltage supply is interrupted. The parameters or the pulse are listed in Table 7. Ri represents the source resistance.

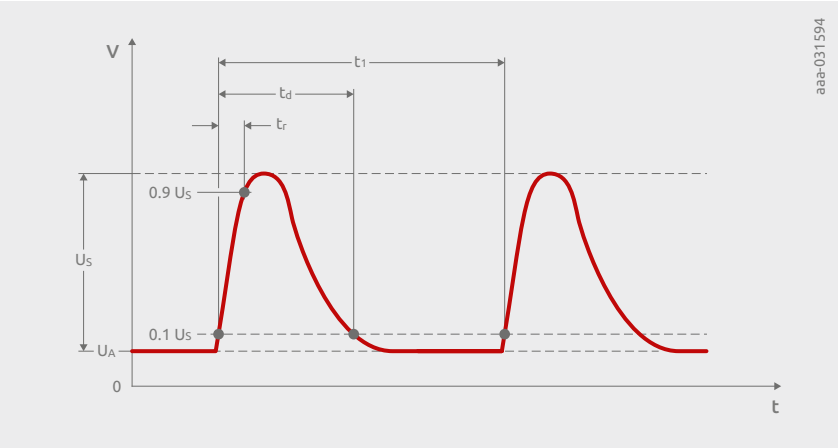


Figure 14 | Waveform of Pulse 2a, interrupted power supply

Table 7: Parameter ranges for Pulse 2a shown in Figure 14

Boad net	U_A (V)	U_S (V)	R_i (Ω)	t_d (ms)	t_r (µs)	t_1 (s)
12 V	13.5 ± 0.5	37 to 112	2	0.05	0.5 to 1	0.2 to 5
24 V	27.0 ± 0.5					

5.8.3 ISO7637-2 Pulse 2b: DC motors as unintended generators

Pulse 2b, shown in Figure 14, represents the effect of an energy sink acting as a source. This can occur e.g. when an electric motor continues to turn after the power supply is shut down. An example is the blower fan and or the windshield wipers. When the ignition is turned off the ground potential remains moving for some time and, in this moment, the electric motor acts as a generator. The parameters for the pulse are listed in Table 8. Ri represents the source resistance.

Table 8: Parameter ranges for Pulse 2b shown in Figure 15

Boad net	U_A (V)	U_S (V)	R_i (Ω)	t_d (ms)	t_r (ms)	t_{12} (ms)	t_6 (ms)
12 V	13.5 ± 0.5	10	0 to 0.05	0.2 to 2	1 ± 0.5	1 ± 0.5	1 ± 0.5
24 V	27.0 ± 0.5	20					

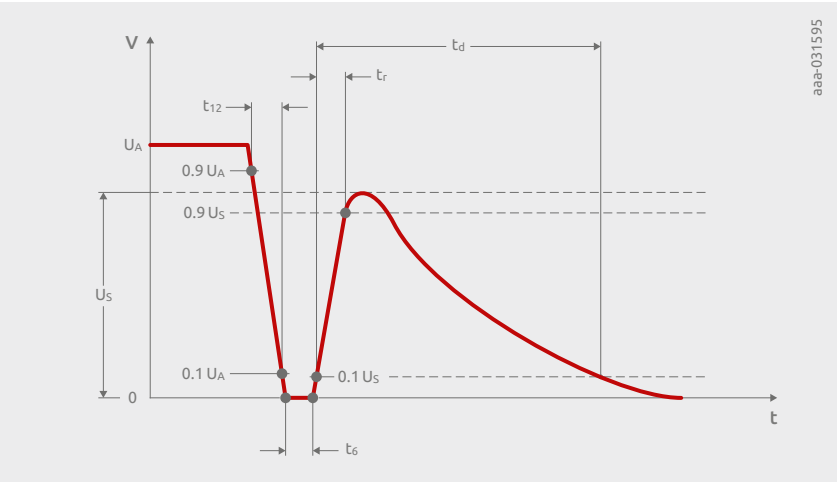


Figure 15 | Waveform of Pulse 2b, DC motors as unintended generators

5.8.4 ISO7637-2 Pulse 3a and 3b: Fast transients

Pulse 3a and 3b represent fast transients in the power supply of the DUT. Pulse 3a represent the negative and pulse 3b positive polarity. See Figure 16 and Figure 17 for the pulse waveforms. These transients can occur every time when electrical load is switched on or off. The connected wiring harness and its parasitic inductance and capacitance or the bouncing of a relay or switch a cause very fast voltage peaks on the supply line. Compared to Pulses 2a and 2b, this pulse is much faster with a higher amplitude Us but lower energy. Occasionally, robustness against these pulses is also requested for external ESD protection devices for CAN or LIN interfaces. The parameters are listed in Table 9. Ri represents the source resistance.

Table 9: Parameter ranges for Pulses 3a and 3b shown in Figures 14 and 15

Boad net	Pulse	U_A (V)	U_S (V)	R_i (Ω)	t_d (ns)	t_r (ns)	t_1 (µs)	t_4 (ms)	t_4 (ms)
12 V	3a	13.5 ± 0.5	-112 to -220	50	150 ± 45	5 ± 1.5	100	10	90
12 V	3b	13.5 ± 0.5	75 to 150						
24 V	3a	27.0 ± 0.5	-150 to -300						
24 V	3b	27.0 ± 0.5	150 to 300						

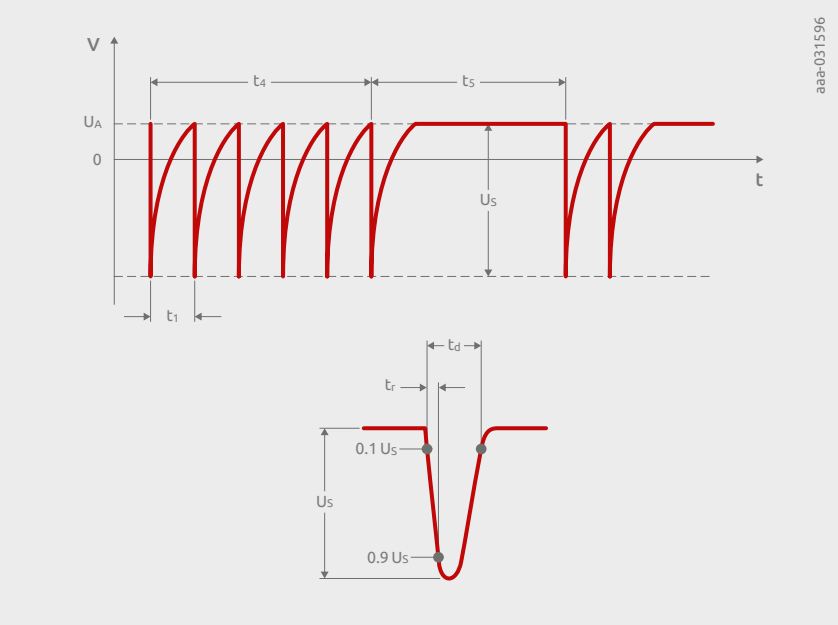


Figure 16 | Waveform of Pulse 3a, negative fast transient

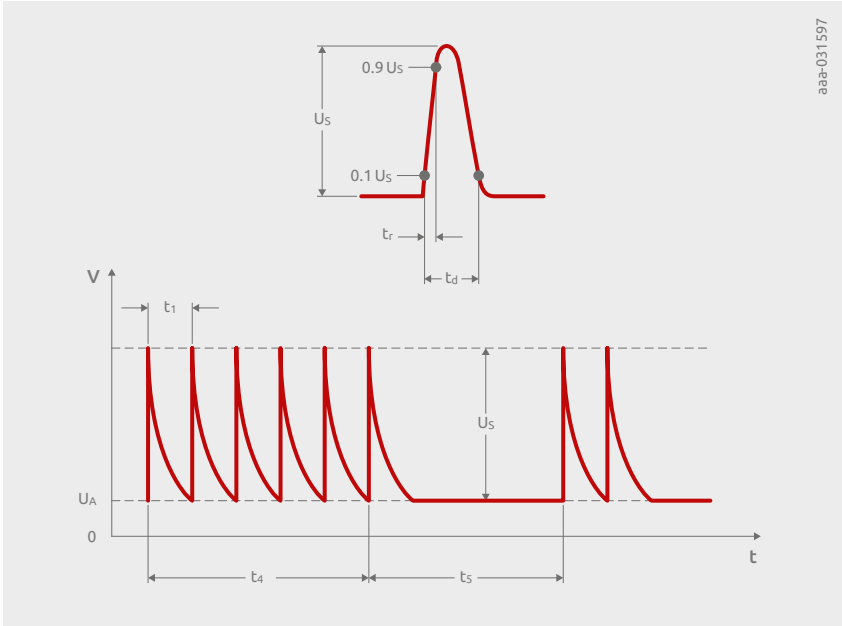


Figure 17 | Waveform of Pulse 3b, positive fast transient

5.8.5 ISO16750-2 §4.3 Overvoltage

When jumpstarting a car significantly higher voltages than the nominal supply voltage can be applied. As all ECUs are supplied from the same source, all systems of the car need to be able to withstand these over voltages. In a 12 V system the DUT has to withstand 24 V for 60 ± 6 seconds and in a 24 V system 36 V for 60 ± 6 seconds. This test is also performed 20°C below maximum operating temperature.

5.8.6 ISO16750-2 Load Dump

The load dump simulates the effect of an empty batterie which is disconnected while charging. An empty battery is charged by the alternator with a comparatively high current. If the battery is disconnected from the supply line during charging, the alternator will produce a voltage peak in the supply line. Two slightly different pulses can occur. These test pulses have previously been published as pulse 6a and 6b in ISO7637-2 and have been shifted to ISO16750-2 later. The first pulse, see Figure 18a, simulates the voltage peak without suppression.

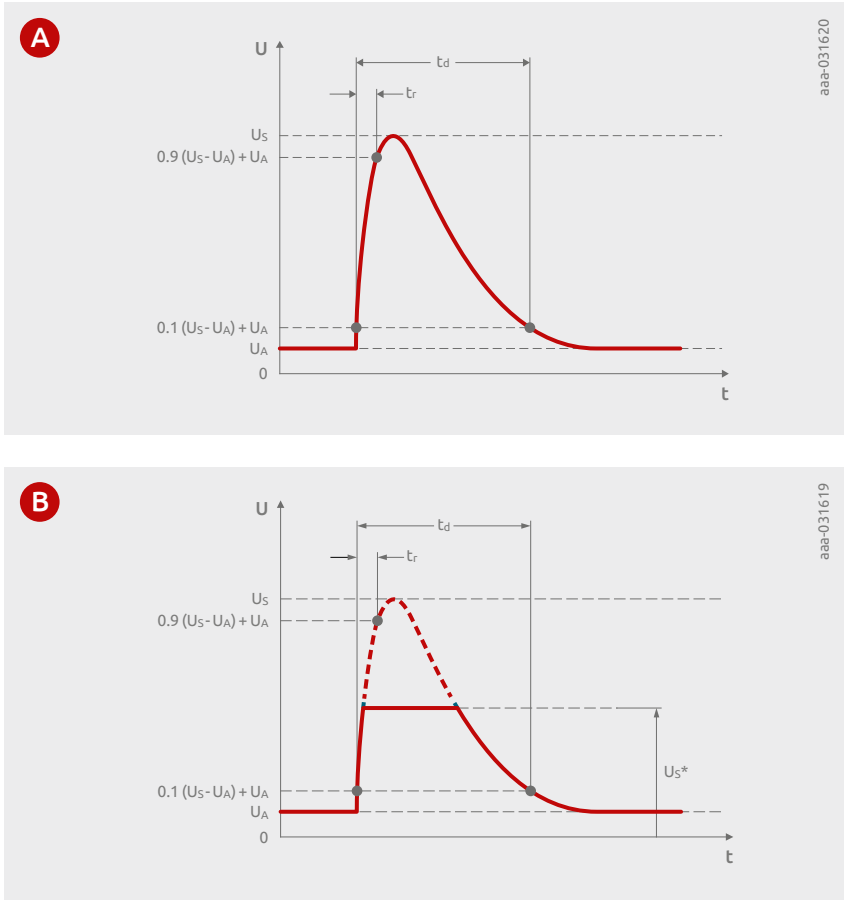


Figure 18 | Waveform of load dump without (A) and with (B) suppression according to ISO16750-2

Figure 18b shows the pulse with a load dump suppression. In this case, the pulse is limited to the value Us* by a centralized load dump suppression. This can be implemented by using a large TVS diode. The parameter range is listed in Table 10. Ri represents the source resistance.

Table 10: Parameter range for load dump shown in Figure 18

Boad net	Pulse	U_S (V)	U_S* (V)	R_i (Ω)	t_d (ms)	t_r (ms)
12 V	5a	79 to 101	–	0.5 to 4	40 to 400	5 to 10
12 V	5b		35			
24 V	5a	151 to 202	–	1 to 8	100 to 350	
24 V	5b		65			

5.8.7 ISO21780 for 48 V board net

New developments in the car architecture consider some alternative board nets such as 48 V to improve overall energy efficiency. The 48 V board net is already introduced in some car concepts and even in series production [10]. This ISO21780 [9] standard describes the requirements and tests for road vehicles with a board net of 48 V including the voltage ranges, slow voltage transients and fluctuations. There are 16 pulses included in the standard and some of them are just adapted from the ISO16750-2 such as the load dump. However, some of the tests are relevant for ESD protection devices due to a risk for a double fault as mentioned above. Since the time duration of these tests are in the range of milliseconds or even seconds, the ESD device placed on the interface will not survive this pulse. ESD device selection should be done with care. In detail it means, that the V_{RWM} should be higher than the maximum voltage of the pulses. As listed in Table 11 load dump and the short term overvoltage are both up to 70 V. The ESD device should have an V_{RWM} > 70 V. To overcome the risk of latch-up also the holding voltage Vh > should be above 70 V.

Table 11: Maximum voltage for the pulses defined in the ISO 21780

Test		Vmax and time duration
01	Nominal voltage range	52 V for 60 s
02	Lower and upper transitory voltage ranges	54 V for 60 s
03	Short term overvoltage	70 V for 40 ms
04	Load dump	70 V for 40 ms
05	Starting profile	
06	Long term overvoltage	60 V
07	Overvoltage with consumer components which may supply electrical energy	58 V
08	Decrease and increase of supply voltage	54 V
09	Voltage ripples	54 V
10	Reinitialization	34 V for ≥ 10 s
11	Discontinuities in supply voltage	48 V
12	Ground loss	52 V
13	Fault current	70 V
14	Ground offset	52 V
15	Short circuit in signal line and load circuit	52 V for 60 s
16	Quiescent current	48 V

5.9 TLP (Transmission Line Pulse) testing

TLP is a comparatively new measurement technique used to characterize complete interfaces or ESD protection components [11][12].

TLP is a short-duration rectangular pulse in a controlled impedance environment of 50 Ω, which improves test accuracy and measurement reproducibility. TLP characterizes performance attributes of devices under stresses that have a short pulse width and fast rise time. Low duty cycles prevent heating.

The TLP test environment shown in Figure 19 can be described as follows: a generator charges a 50 Ω transmission line with a pre-adjusted voltage. Once the switch is closed, the energy is applied to the DUT. The current into the DUT is measured by a current probe, while the voltage at the DUT is monitored using a high-speed oscilloscope. The pulse length, rise, and fall times can be changed at the generator. Typically, the standard pulse applied has a 100 ns duration and rise and fall times of 1 ns each. The minimum programmable transition times are 100 ps.

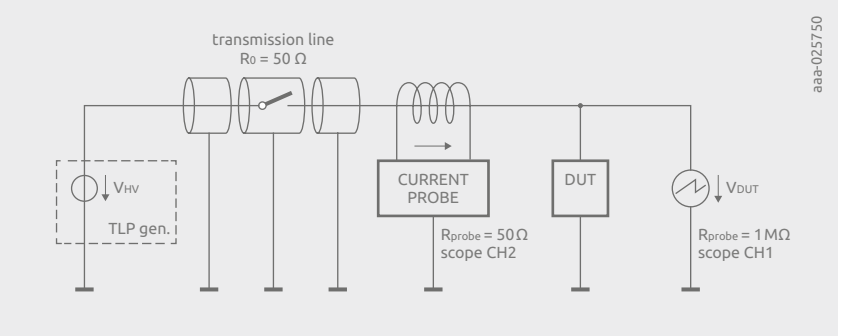


Figure 19 | TLP test set-up

The TLP test is performed starting gradually from low pulse voltages to higher voltages, with a pre-defined step width. In Figure 20 the TLP measurement voltage and current traces are depicted. The voltage and current samples are averaged for a window of 20 ns. The temporal window is located from 70 ns to 90 ns within the 100 ns test pulse, the window-based method eliminates noise. Also, the window's location ensures that the system is settled so that run-in effects like overshoots are eliminated. Each measurement result pair of voltage and current becomes a point on the TLP graph that shows a TLP I-V characteristic, i.e. the TLP-curve. Due to the rather late averaging window, a TLP curve itself does not inform how fast a snap-back device turns on or how big potential overshoots are. It is necessary to have a detailed look at the voltage waveforms to judge the overshoot and turn-on behavior of an ESD protection device.

The steepness of the TLP curve ΔV/ΔI is the R_{dyn}, which is an important parameter for selecting ESD and surge protection devices.

TLP testing can be done with ESD protection devices, and with interface pins of complete systems with and without ESD protection. From the derived TLP curves conclusions can be drawn about which protection device is suitable to protect a product safely and reliably.

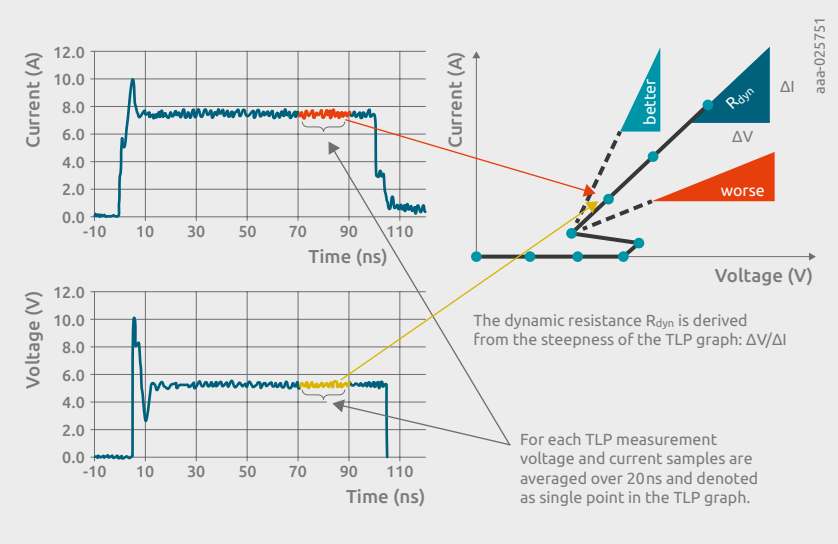


Figure 20 | TLP curve derived from a TLP test event

5.10 VF-TLP (Very Fast-TLP) testing

A similar testing method to TLP is Very-Fast TLP (VF-TLP) [13]. The major differences are the 1 ns to 10 ns duration of the test pulses and the short rise and fall times of 100 ps to 600 ps.

Figure 21 shows the VF-TLP measurement set-up. Due to short pulses, the current is not measured with a current probe. Instead, it is derived from measuring incident and reflected voltages separately with an oscilloscope. This is done in a similar way to time domain reflection (TDR) measurement. The current in the DUT is calculated using:

$$I_{DUT} = I_{incident} + I_{reflected} = \frac{V_{incident} - V_{reflected}}{50\ \Omega}$$

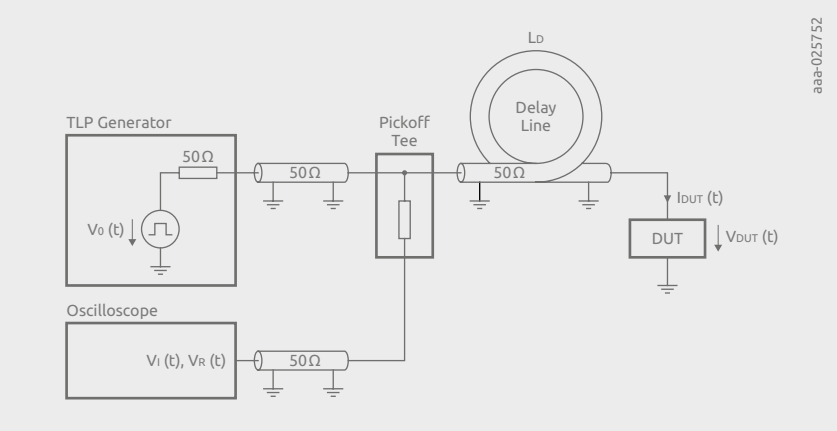


Figure 21 | Test set-up for VF-TLP measurement

In conclusion, VF-TLP tests provide a good indication for determining the switching speed of ESD protection devices. The small pulse length is useful because the impact of the first overshoot of an ESD event on a target system can be investigated.

In contrast, the 100 ns standard TLP pulses are roughly equivalent to the energy of a complete ESD pulse, in which the larger proportion of energy is carried in the wider second shoulder of the pulse.

Some SOCs can be damaged by the first overshoot peak current of IEC61000-4-2 pulses, others may be destroyed by the overall amount of energy. To select an appropriate ESD protection device it is important to understand which mechanism damages an interface - the first overshoot of an ESD strike or the entire pulse with the pulse energy.

5.11 HMM (Human Machine Model) testing

Testing with ESD guns as defined in IEC 61000-4-2 was originally for single electronic components. The limitations and disadvantages of this testing method are discussed in Section 5.2. The biggest problem is the limited reproducibility and quite large spread in the waveform of ESD guns. The first short overshoot spike of the nominal waveform is most problematic, as is aging of high-voltage relays in the guns. Testing with open ESD guns creates a great deal of EMI interference. ESD guns can even spoil other measurements in a laboratory via uncontrolled and unshielded electromagnetic radiation and interference via ground connections. Datasheets of ESD protection components often show clamping curves for ESD gun discharge experiments with different voltage levels. The test results depend a lot on the set-up of the measurement such as DUT test fixtures, the way in which the ESD gun is connected and the level of undesired reflections occurring since there is no consistent characteristic impedance being used for the whole measurement set-up. Therefore, it is hard to compare clamping test results if different test laboratories have been used.

HMM generators deliver a signal waveform identical to ESD gun generators but with a 50 Ω termination. Therefore standard 50 Ω coaxial cables can be used. There is no uncontrolled significant radiation of high frequency electrical and magnetic fields. Tolerances for the waveform accuracy are much tighter at +/−10%.

Many TLP test generators offer an HMM signal waveform as an alternative to 50 Ω terminated rectangular transmission line pulses. HMM testing delivers reliable and reproducible test result and should replace testing with ESD guns. Like TLP and VF-TLP test results, clamping waveforms from this test method do not depend on a test location and small differences in the test implementation regarding shielding, DUT implementation and grounding. They are very beneficial for the selection of a suitable ESD protection for sensitive super-speed interfaces like USB 3/4, HDMI 2.1 or DVI ports.

References

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Chapter 6

RF measurements, signal integrity and testing methods

6.1 S-parameters, S-parameter models

Scattering parameters, also known as S-parameters, reflect the electrical behavior of a network in a black box like the one shown in Figure 1, and are particularly useful for higher frequencies. They describe how the energy distributes in a network and are widely used to describe the small signal behavior of linear devices and networks[1]. The behavior of the device under test (DUT) is stored in a standardized file format called Touchstone.

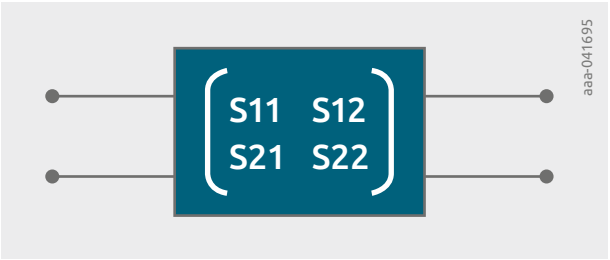

Figure 1 | S-parameter box of a two-port network analyzer

A particular advantage of S-parameters is that they can be easily stacked and combined with discrete elements in a circuit simulation. This is useful for system design and can be applied to all elements in the system that are relevant to RF behavior or high-speed data transmission. Only the S-parameters of related components like connector, cable, filter, ESD-protection diodes etc. must be available.

During the characterization of the DUT, a network analyzer (NWA) is connected to the DUT and energy waves applied to the pins of the DUT. The combined inputs and outputs of the NWA are known as ports and are where the transmission and reflection of the excited waves is measured. The format and naming of the resulting Touchstone file depends on the number of characterized pins. The most common file formats are s1p, s2p and s4p, because most NWAs are limited to a maximum of four ports, but analyzers with a higher port count are also available (eight ports, for example). The number of entries in the stored matrix inside the Touchstone file depends on the port count used for the measurements. For a s2p file, as shown in Figure 1, the matrix consists of four entries while for a s4p file like that shown in Figure 3, 16 matrix entries are needed.

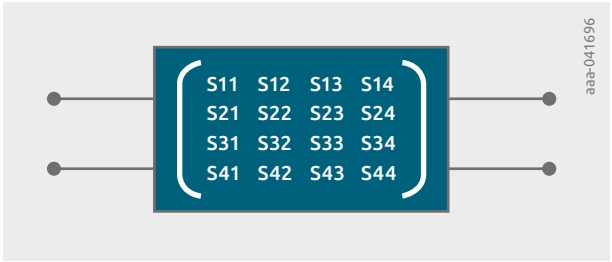

Figure 2 | S-parameter box and matrix of a four-port network analyzer

S-parameters can also be created in simulation. This can be done in schematic based or electromagnetic analysis. Here the theoretical port count is almost infinite.

6.1.1 General single-ended S-parameter setup and content

The standard measurement setup for ESD protection devices characterizes the DUT as in the actual application as a shunt to GND. A schematic of the setup for a two-port measurement is shown Figure 3. In Figure 4, a standard s4p measurement set-up is shown. Interestingly, the layout used by the NWA manufacturer Rohde & Schwarz differs slightly from the common standard, as shown in Figure 5, switching port 2 and port 4.

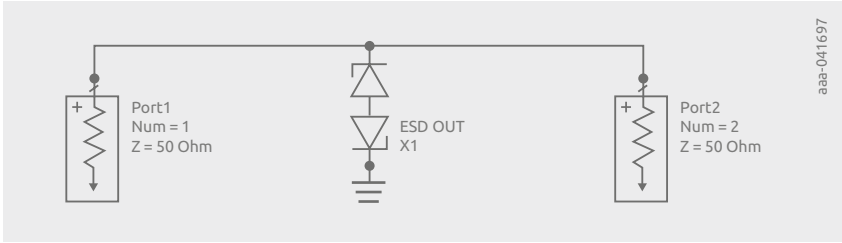

Figure 3 | Two-port S-parameter measurement setup

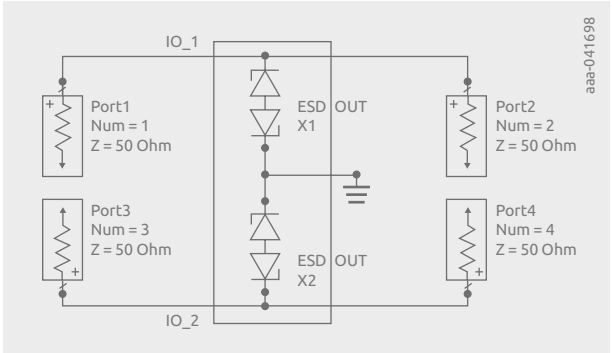

Figure 4 | Standard four-port S-parameter measurement setup

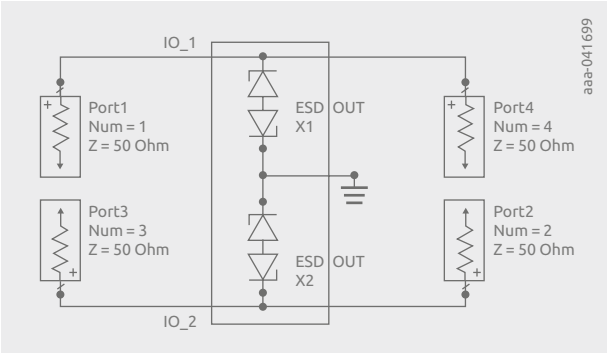

Figure 5 | Standard four-port S-parameter Rohde & Schwarz measurement setup

In Figure 6, the principal flow of the four different kinds of signals during an s4p measurement can be seen. The insertion loss (IL) is the signal transmission through the DUT, while the return loss (RL) gives the portion of the signal that is reflected at the IOs. If more than two ports are used to characterize the DUT, the crosstalk between the IOs can also be investigated. The crosstalk of neighboring ports is known as near-end crosstalk (NEXT) and the crosstalk of ports on opposite sides as far-end crosstalk (FEXT).

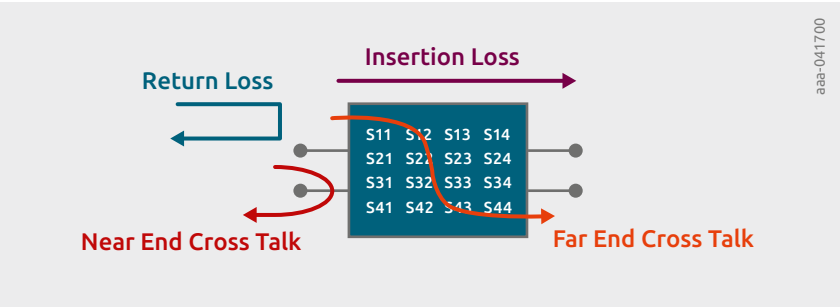

Figure 6 | S-parameter signal flow characterization

The information stored in the S-parameters obtained using the setups in Figures 3, 4 and 5 is usually named as shown in Table 1.

Table 1: S-parameter information

	Two port	Four port	Four port (Rohde & Schwarz)
Transmission	S21, S12	S21, S12 S43, S34	S41, S14 S23, S32
Reflection	S22, S11	S22, S11 S44, S33	S44, S11 S22, S33
Crosstalk	not applicable	S31, S32, S13, S14 S41, S42, S23, S24	S31, S34, S13, S12 S21, S24, S43, S42

For better understanding of the device or system, the S-parameters can be visualized in frequency-dependent plots. The insertion loss (IL) graph shown in Figure 7 illustrates how much of a signal will pass the DUT. This information is stored in S21 and S12.

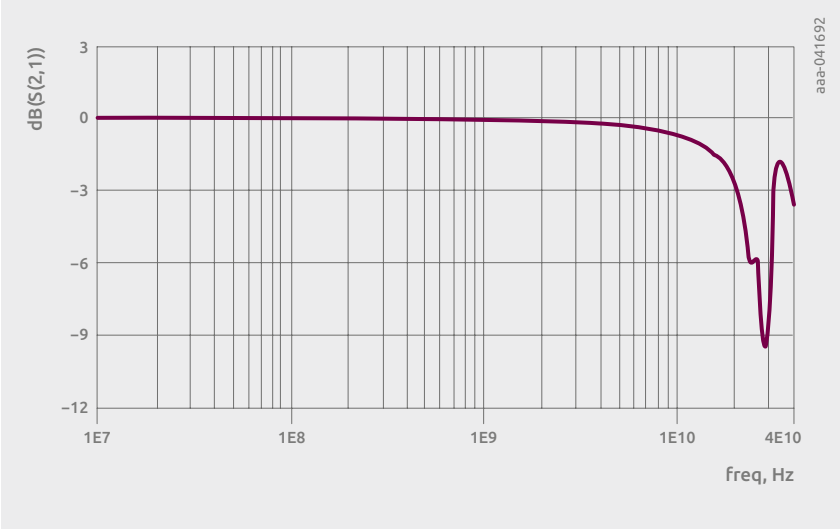

Figure 7 | Insertion loss graph

The return loss (RL) can be seen in Figure 8 and visualizes how much of a signal will be lost due to reflection at the device over the examined frequency range.

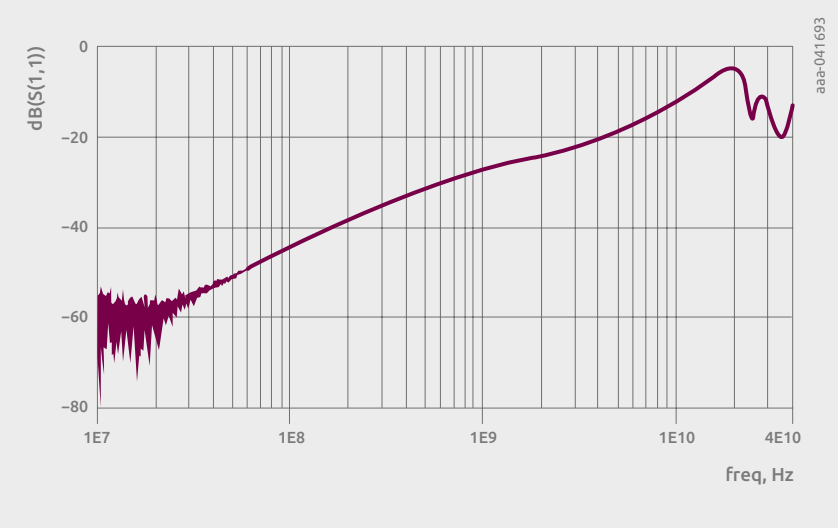

Figure 8 | Return loss

Finally, a crosstalk (XT) graph like the one shown in Figure 9 gives an indication of how much of the signal will be transferred to the wrong port due to factors such as inductive and capacitive coupling. Usually, it differentiates between far-end crosstalk (FEXT) and near-end crosstalk (NEXT).

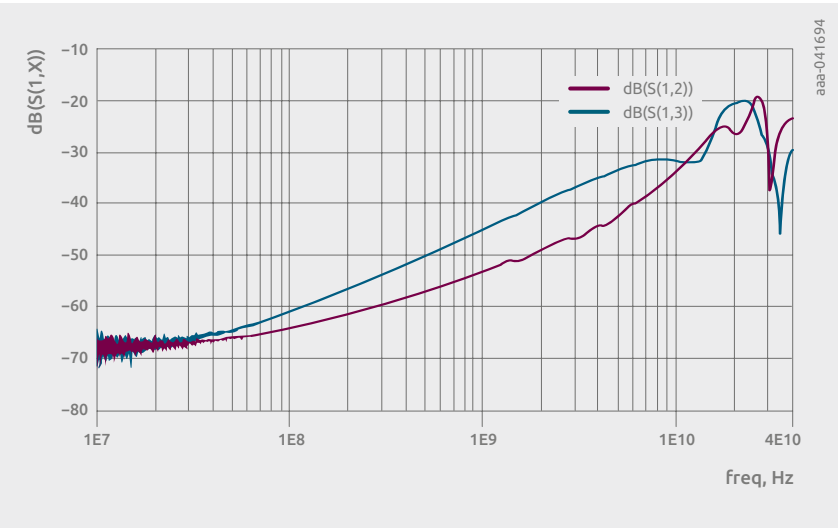

Figure 9 | Crosstalk graph

Single-ended S-parameters of passive networks under ideal conditions are symmetric, passive and causal. For small-signal analysis, ESD protection devices are considered passive.

Symmetry	Sij=Sji
Passivity	No amplification, all values ≤ 0 dB
Causality	Means that the response does not precede the excitement of the DUT. When testing for causality, if the causality condition is set too harsh, measurement noise can make a DUT appear non-causal.

6.1.2 Calculate mixed-mode S-parameters from single-ended S-parameters

One way in which it has become possible to achieve faster data transfer rates without losing information in recent years has been by using differential protocols. To develop and verify a system with respect to differential signals, differential ports can be used or a single-ended characterized system converted to mixed mode.

A set of mixed-mode S-parameters consists of common-mode, differential-mode and mode-conversion parts.

Single-ended S-parameters			
IL/RL		NEXT/FEXT	
S11	S12	S13	S14
S21	S22	S23	S24
NEXT/FEXT		IL/RL	
S31	S32	S33	S34
S41	S42	S43	S44

è

Mixed-mode			
Differential-Differential		Common-Differential	
SDD11	SDD12	SDC11	SDC12
SDD21	SDD22	SDC21	SDC22
Differential-Common		Common-Common	
SCD11	SCD12	SCC11	SCC12
SCD21	SCD22	SCC21	SCC22

Using the port setup shown in Figure 4, S-parameters can be converted to mixed-mode using the following equations

For pure differential-mode signals:

$$SDD11=0.5*(S(1,1)-S(1,3)-S(3,1)+S(3,3))$$
$$SDD12=0.5*(S(1,2)-S(1,4)-S(3,2)+S(3,4))$$
$$SDD21=0.5*(S(2,1)-S(2,3)-S(4,1)+S(4,3))$$
$$SDD22=0.5*(S(2,2)-S(2,4)-S(4,2)+S(4,4))$$

Most important for differential signaling is SDD21, which provides information about how much of the differential signal excited at Port 1 can be detected on the output Port 2.

For pure common-mode signals (as ESD events are usually considered):

$$SCC11=0.5*(S(1,1)+S(1,3)+S(3,1)+S(3,3))$$
$$SCC12=0.5*(S(1,2)+S(1,4)+S(3,2)+S(3,4))$$
$$SCC21=0.5*(S(2,1)+S(2,3)+S(4,1)+S(4,3))$$
$$SCC22=0.5*(S(2,2)+S(2,4)+S(4,2)+S(4,4))$$

Differentially excited systems convert parts of the signal to common mode and exciting the system with common modes will lead to part of it being converted to differential mode.

Differential to common mode:

$$SCD11=0.5*(S(1,1)-S(1,3)+S(3,1)-S(3,3))$$
$$SCD12=0.5*(S(1,2)-S(1,4)+S(3,2)-S(3,4))$$
$$SCD21=0.5*(S(2,1)-S(2,3)+S(4,1)-S(4,3))$$
$$SCD22=0.5*(S(2,2)-S(2,4)+S(4,2)-S(4,4))$$

Common mode to differential mode:

$$SDC11=0.5*(S(1,1)+S(1,3)-S(3,1)-S(3,3))$$
$$SDC12=0.5*(S(1,2)+S(1,4)-S(3,2)-S(3,4))$$
$$SDC21=0.5*(S(2,1)+S(2,3)-S(4,1)-S(4,3))$$
$$SDC22=0.5*(S(2,2)+S(2,4)-S(4,2)-S(4,4))$$

If single-ended S-parameters are used in the transient channel simulation, it will be simulated correctly without any transformation being required, as long as the ports are connected correctly.

6.1.3 The measurement setup

Depending on product performance and package, Nexperia recommends measuring S-parameters in three principal set-ups:

- Direct contact on die with ACP probes.
- Contact on adapting PCB without de-embedding.
- Contact on adapting PCB with de-embedding.

Direct contact on die with ACP probes

In Figure 10, probes which are connected to an NWA are directly in contact with a product. This set-up is often used for two-pin products which have only a small bandwidth. The frequency range of this measurement is from 300 kHz to 18 GHz and the result is stored in a s2p file.

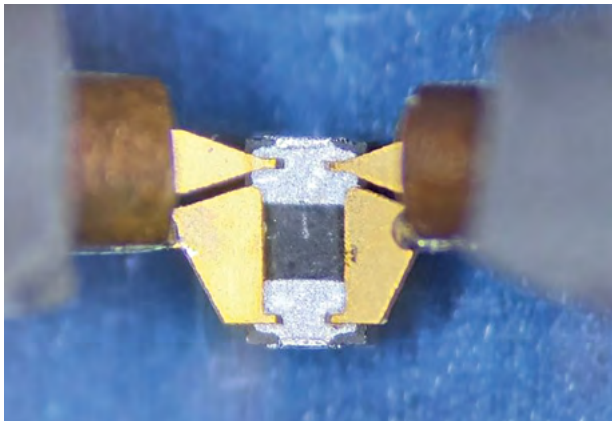

Figure 10 | ACP needles in direct contact with a product

Contact on adapting PCB without de-embedding

Due to increasing data rates, the bandwidth of ESD protection devices needs to be higher and characterization carried out up to higher frequencies. The set-up shown in Figure 11 offers measurements up to 40 GHz, starting at 10MHz. The disadvantage is that device characterization includes a small piece of adapting PCB.

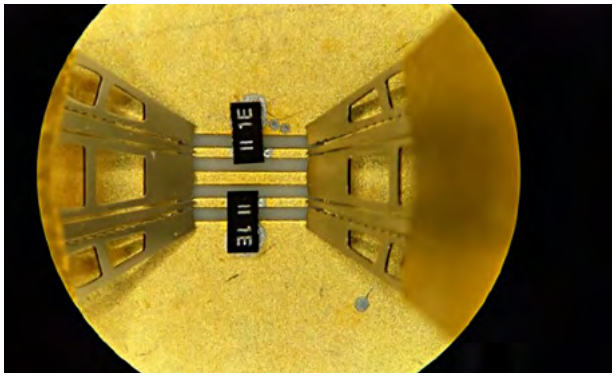

Figure 11 | Z-probes DUT on PCB

Contact on adapting PCB with de-embedding

The pure data of the device can be calculated using a methodology called de-embedding. For this method, a set of specific calibration structures is needed to subtract the PCB from the measurement data. This setup is shown in Figure 12. The resulting S-parameters are s2p files containing only the device behavior and are currently available for the frequency range from 1GHz to 40GHz. This measurement method is newly implemented and not yet rolled out for all low-capacitance devices, but in general is available for SOD962-2 and SOD882 packages. More details can be found in Chapter 6.2.

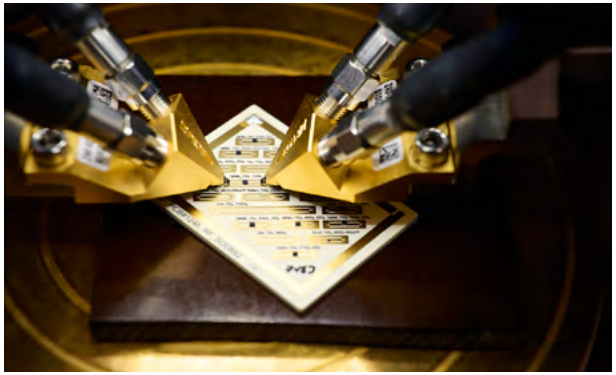

Figure 12 | De-embedding PCB and Z-probes

6.1.4 The Touchstone file

The Touchstone format was created by HP in 1984 and is well defined since it was specified in the IBIS project[2]. Today it is industry standard for circuit simulation and measurement equipment[3]. It contains a header describing what kind of data is inside. Nexperia usually shares *.s2p and *.s4p files. Comments are often used to share more details about the set-up and indicated by an exclamation mark, '!'.

The basic elements on the top of the *.snp file that can be opened in most text editors could look like

#	Hz	S	RI	R 50.0

#	is the key for the header start
Hz	gives the unit of the frequency. Also possible are GHz, MHz, kHz and Hz. Default: GHz
S	specifies which kind of parameters are contained in the file. Nexperia usually shares S-parameters, which is also the default value, but Y, Z, H, G are other network parameters you may find inside *.snp files.
RI	defines the format of the number pairs in the file. In this case it is RI which is the real-imaginary format. Other possible entries are MA (magnitude angle) and DB (dB angle). Whatever format is used, standard circuit simulation tools will convert the data to the appropriate output format.
R 50	R is a keyword and indicates the used reference resistance of the present network parameters. In this case it is 50 Ohms.

Example standard s4p:

```
# HZ   S   RI   R     50.00
! Rohde & Schwarz ZVA/B
! Build by IDs Lab - nodal (TOUCHSTONE FILE SPECIFICATION):
! Frequency S11 S12 S13 S14
! S21 S22 S23 S24
! S31 S32 S33 S34
! S41 S42 S43 S44
!
!
1.000000E+7 0.001160 0.000419 -0.000316 -0.000176 0.000471 2.814109E-5 0.998984 -0.005751
   -0.000276 1.848257E-5 0.000610 0.000912 1.000381 -0.000303 0.000282 0.000229
   0.000448 7.781532E-5 0.998782 -0.005097 0.000340 -0.000495 -0.000246 -8.026873E-5
   0.998467 -0.006501 0.000340 0.000201 -0.000357 1.457439E-6 9.974651E-5 0.000852

1.002769E+7 0.000708 -0.000682 -0.000346 -6.352049E-5 0.000329 0.000108 1.004546 -0.002391
   -0.000375 -7.856413E-5 -5.582220E-5 -0.000434 0.999443 -0.002929 0.000302 0.000103
   0.000439 0.000182 1.001549 -0.004035 0.000494 -0.000354 -0.000219 -0.000135
   1.000727 0.000962 0.000349 8.651197E-5 -0.000381 -0.000174 -0.000332 -0.000189

   ...

3.988957E+10 0.273262 0.232473 0.011925 0.012870 -0.101284 -0.017386 -0.392301 0.725783
   0.012520 0.012486 0.291126 0.176408 -0.385907 0.750851 -0.097811 -0.020169
   -0.100614 -0.020228 -0.419647 0.725836 0.274159 0.217793 0.011720 0.013681
   -0.394284 0.734390 -0.097466 -0.021181 0.012938 0.011775 0.309988 0.175594

4.000000E+10 0.276777 0.229691 0.012631 0.014085 -0.101508 -0.015867 -0.383324 0.731174
   0.012361 0.011878 0.295442 0.172470 -0.371234 0.755145 -0.099194 -0.019707
   -0.101984 -0.018054 -0.406129 0.729122 0.276818 0.214032 0.013991 0.012038
   -0.381065 0.739879 -0.098687 -0.020620 0.013467 0.011393 0.312831 0.171962
```

Figure 13 | Standard s4p file for ESD protection devices

1 Touchstone file - Wikipedia
2 http://www.ibis.org/connector/touchstone_spec11.pdf
3 Touchstone file - Wikipedia

6.2 De-embedding the PCB

As data transmission protocols evolve the frequencies of transmitted signals become ever higher, increasing the need for every part of the signal path to produce as little disturbance as possible. Nexperia is continuously improving its products so that their impact on the transmitted signal is minimized. This also applies to the signals that are intended to measure a device's performance. The impact of the device becomes smaller and smaller compared to the impact of the environment and the measurement set-up. Weaknesses in measurement techniques that were once state of the art first become visible, then problematic.

6.2.1 The classic methods

The three methods Nexperia uses for S-parameter measurements are described in Chapter 6.1.2. The oldest is direct contact of the DUT with ACP probes. With this method the calibration is performed on the impedance standard substrate supplied by the probe manufacturer. This sets the reference plane onto the probe tip, which is ideal for DUT characterization without further de-embedding. Unfortunately, this method also has downsides. The first is that a suitable probe size is needed for every package in the portfolio. For large packages or those that have a more complicated pin layout, no probes are available. Another downside is poor repeatability – a slight change in contact pressure changes results quite significantly. The third and most significant downside is that for frequencies above 8 GHz the measurement results diverge more and more from what can be expected from DUT physics (insertion loss values inexplicably improve, for example). The lower the insertion loss of the DUT, the greater the relative error created by the ACP probes. This characteristic effect of the ACP probes can be seen on datasheets for high-speed ESD protection devices industry wide. This is why we do not prefer this method for characterization of high-speed devices anymore.

To alleviate some of these downsides, a combination of more sophisticated |Z| probes and small adapter PCBs is used. Compared to the ACP probes, |Z| probes are specified for higher frequencies up to 40 GHz. Like the ACP probes, they are calibrated on an impedance standard substrate from the probe manufacturer. Their symmetry and overall improved design yield good results over a wide frequency range and show little to no dependence on contact pressure. The use of small adapter PCBs allows us to adapt them to any package without maintaining a large stock of different probe sizes and having to recalibrate when different packages are to be measured in one session. Unfortunately, they come with a new downside, which is that the adapter PCB is part of the measured S-parameters. That is not a significant issue for devices that have large insertion losses on their own. Again, however, the lower the insertion loss of the DUT, the greater the relative error.

6.2.2 The new de-embedding method

To combine the advantages of both of these methods, Nexperia developed its own PCB containing calibration standards as well as footprints for several DUTs. This way, the PCB structures can be easily de-embedded from the S-parameters, and calibration and measurement environment are exactly the same.

Additionally, these PCBs reserve one footprint for a resistor to be used as a T-Check. The T-Check is an accuracy test for the calibration as described by Rohde & Schwarz in their Application Note 1EZ43. More information on the T-Check can be found in Section 6.3.

Different calibration methods can be performed with the given standards on this PCB. For high-frequency precision, experts agree that through-reflect-line (TRL) calibration yields the best results of the available methods. This is confirmed by our T-Check measurements. The main difference between this calibration method and others is the use of one or more line standards instead of a load or match standard. The information needed for calibration is taken from the characteristic impedance of the line instead of the impedance of a lumped element. The lower the desired measurement frequency, the longer the line standard needs to be. A line standard that allows for the measurement band to start at 1 GHz is already in the cm range. Longer standards would make the PCB impractical to handle without relevant gains in precision at frequencies below 1 GHz. In these regions other calibration methods like through-reflect-match (TRM) or through-open-short-match (TOSM) yield good results.

It is important to remember that there is no universal best calibration method. Each one has advantages and downsides. This is why there might be more than one correct set of S-parameters for the same device. Be sure to be precise about your needs when requesting S-parameter measurements.

6.3 T-Check

Testing the accuracy of the calibration of a vector network analyzer can be tricky and subjective. The T-Check provides an objective measure of the quality of calibration by measuring a simple resistor in a T-configuration towards ground (see Figure 14). A number of calculations are then performed using the measured S-parameters. The calculations are based on the fundamental dependencies that a set of passive two port S-parameters is subject to.

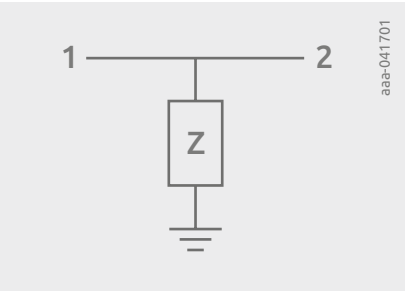

Figure 14 | DUT configuration for a T-Check

The precise calculations and theory can be found in the Rohde & Schwarz Application Note 1EZ43. The result is a unitless number c_T for every frequency step measured. These values can then be plotted over frequency to obtain a clear indication of calibration quality across the entire measurement band (see Figure 15).

With ideal calibration, c_T should be 1. The more the result deviates from this, the poorer the quality of the calibration. The user must decide for themselves what level of deviation they consider not good enough. That being said, a value of, for example, 0.8 does not mean that $|S_{21}|$ deviates from the correct value by 20%. In fact, $|S_{21}|$ could be very precise. All of the information in the set of S-parameters goes into the calculation and it is not possible to draw conclusions for individual values from c_T.

We also need to consider the fact that the insertion and return loss values of our high-speed protection devices are coming close to the tolerance of even high-end VNAs. Two different calibration methods that might reach c_T values of 0.98 and 1.02 respectively are widely considered good but might still lead to significant relative differences in insertion loss values when measuring the same device (0.3 dB V 0.4 dB, for example).

Nevertheless, the T-Check gives us a solid objective indication of whether we may need to recalibrate or – when the deviation persists – change our method of calibration.

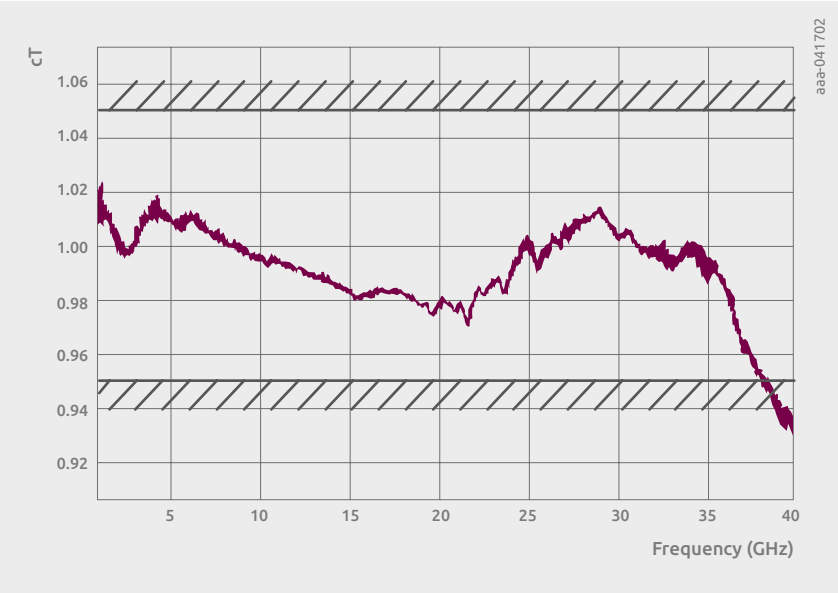

Figure 15 | T-Check example

6.4 High-speed serial data interface

Modern computers and multimedia systems use a variety of data interfaces to communicate with devices such as mice, keyboards, multimedia output (audio and video), printers and data storage devices. Higher video resolutions, larger data volumes and increasing storage capacities require data interfaces with ever faster data rates to display video smoothly on the display or to store and retrieve data quickly on a mass storage device.

Whereas video interfaces for the transmission of video signals with a transmitter (TX) and a display as receiver (RX) work uni-directionally without evaluating the transmission errors, data interfaces such as USB 2.0, USB-C and PCI express are bi-directional. USB 2.0 uses a common data line for RX/TX. The architecture of USB-C/USB 4v2 requires a separate RX input and TX output in the system-on-chip (SOC), which are connected with differential data lines on the PCBs and by cables, as shown in Figure 16.

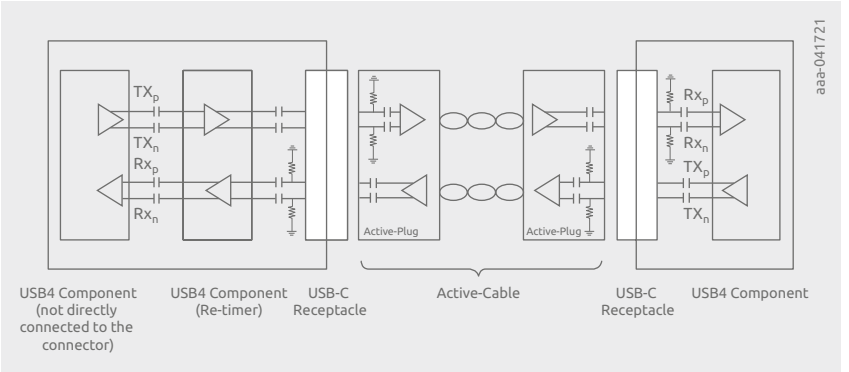

Figure 16 | Schematic representation of a USB 3 and USB 4v2 channel (source: USB-IF)

6.4.1 Graphics interfaces

The best-known graphics interfaces are DVI and its extension HDMI. Both standards transmit video signals using transition-minimized differential signaling (TMDS) coding, and with HDMI the audio signal is also TMDS-coded. Figure 17 shows the basic complete structure of the DVI and HDMI interface, although only the high-speed data lines are considered here.

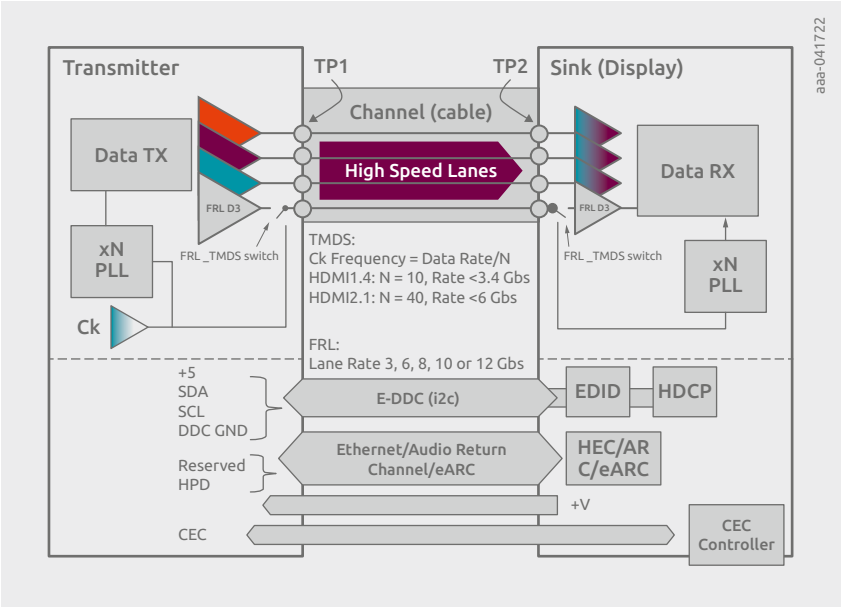

Figure 17 | Schematic representation of a HDMI interface (Source: Keysight)

The HDMI interface has four differential data lines that transmit both TMDS-coded signals at up to 6 GB/s and fixed rate link (FRL) signals.

TMDS uses three lines for video data and one differential line for the pixel clock. With a maximum pixel clock frequency of 340 MHz, the HDMI 1.4b standard can transmit 3.4 GB/s per video channel, which enables a resolution of 1280x720p @ 59.94/60 Hz or 1920x1080i @ 59.94/60 Hz. HDMI 2.0 enabled a pixel clock of 600 MHz and a data rate of 6 GB/s at 4096x2160p @ 60 Hz.

With ever increasing video resolutions, the TMDS protocol was no longer sufficient. To maintain compatibility, the FRL-coded signal is transmitted on the pixel clock and TMDS lines instead of the TMDS-coded signal. This achieves a resolution of 7680x4320P @ 60 Hz at a maximum of 12 GB/s per FRL line. After querying and evaluating the displayable video resolution, the interface can switch between TMDS and FRL.

6.4.2 High-speed serial data interfaces

When it was introduced in 1996, the Universal Serial Bus (USB) already enabled data transfer at 12 MB/s (full speed) and replaced the PS/2 interface by enabling the connection of a mouse and keyboard. Thanks to constant extensions to the USB standard, 480 MB/s (Hi-Speed USB) can be transferred with USB 2.0. With USB 3.0 (SuperSpeed), the USB interface enables the transmission of data rates of 5 GB/s, 10 GB/s and 20 GB/s, which requires an extension of the USB interface with additional RX and TX data lines. The prerequisite for this is that the USB interface remains downward-compatible with USB 2.0 and USB 1.0. Table 2 shows the development of the USB standard.

One innovation has been the introduction of USB-C. Despite its small design, the connector has 12 contacts on both sides and can be plugged in in any direction. Figure 18 shows the contacts in a USB-C plug with contact rows A and B. The high-speed serial data interface contacts USB 1.x and USB 2.0 are represented by D+ and D- and RX1/TX1 or RX2/TX2 for USB 3.x and USB 4.x.

The parallel use of more than two data line pairs already enables a data rate of 40 GB/s with USB 4v1. With USB 4v2, the signal is modulated PAM-3 (pulse amplitude modulation Level 3). This enables a data rate of 80 GB/s.

The ability of USB-C to transfer PCIe, DisplayPort and Thunderbolt 3 in addition to USB 3.x meant an upgrade to higher transfer rates was necessary.

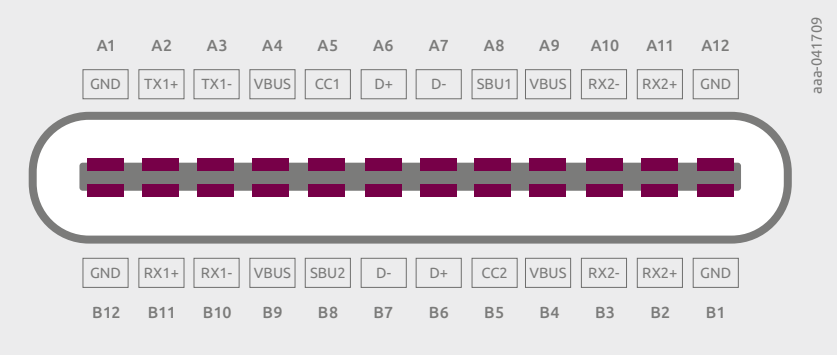

Figure 18 | Contacts of a USB-C receptacle

Table 2: USB standards (Source: Wikipedia and USB-IF)

Mode	Year	Designation	Current Naming	Speed	Plug
USB 1.0/1.1	1996/1998	USB 1.0/1.1	Full-Speed	12 MB/s	diverse
USB 2.0	2000	USB 2.0	Hi-Speed USB	480 MB/s	diverse
USB 3.0	2008	USB 3.2 Gen 1x1	SuperSpeed USB	5 GB/s	diverse
USB 3.1	2013	USB 3.2 Gen 2x1	SuperSpeed+ USB 10 GB/s	10 GB/s	diverse
USB 3.2	2017	USB 3.2 Gen 2x2	USB 20 GB/s	20 GB/s	USB-C
USB 4	2019	USB 4 1.0	USB 40 GB/s	40 GB/s	USB-C
USB 4v2	2022	USB 4 2.0	USB 80 GB/s	80 GB/s	USB-C

6.4.3 ESD-Protection

As the data rate increases, the structure widths of the integrated circuits in a data link become smaller and smaller and therefore more susceptible to damage from ESD. To increase robustness, an ESD diode is placed on each signal line, e.g. near the connector, in addition to the ESD protection implemented in the SOC.

Figure 19 shows a possible application of several ESD diodes in a data interface with connector, data lines and integrated circuit (IC). The signal is fed into the system via the connector and routed to the SOC via the impedance-controlled differential lines. In the signal path, the contacts of the connector, the ESD diodes, the vias and the contacts of the SOC represent discontinuities that influence the impedance curve in such a way that unwanted reflections occur, which can have a strong impact on signal integrity. These reflections lead to signal degradation due to greater amplitude and time jitter in the channel and a resulting higher bit error rate, which in the worst case can render the data signal unusable.

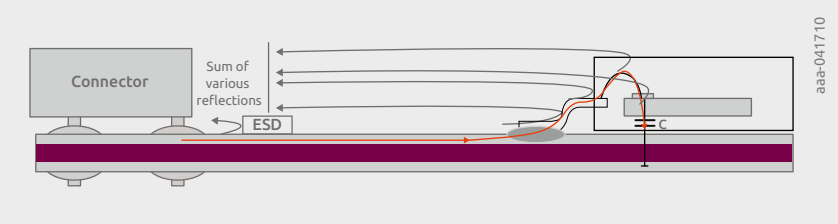

Figure 19 | ESD diode applied to interface

6.4.4 Time domain reflectometry

Because the ESD diode influences the signal integrity through reflection, the selection of the component is of immense importance. It is essential that its parasitic elements influence the signal as little as possible and maintain signal integrity. This requires the ESD diode to be as small as possible and have a low parasitic capacitance. The properties of an ESD diode on a data line can be quickly assessed using time-domain reflectometry (TDR) measurement.

Figure 20 illustrates the basic measurement set-up of a TDR measurement system without a device under test (DUT). The core of the 50 Ω based system is a voltage source that feeds a pulsed square-wave signal, also known as a stimulus, with a defined amplitude into the line. The rise time of the source is adjustable and can therefore be adapted to the interface under investigation. The TDR signal is visualized in an oscilloscope linked to the measuring system. Note that the pulse reflection is evaluated in the measuring system and the signal with the running and reflected wave has twice the propagation time.

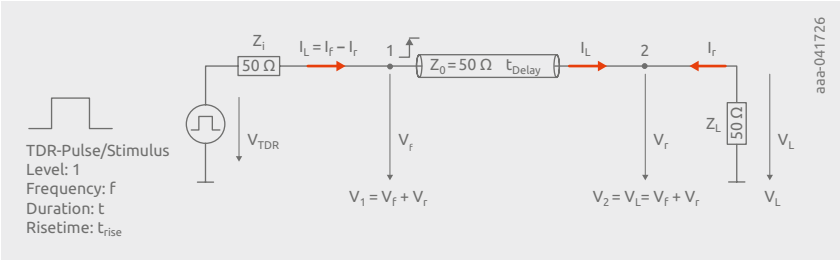

Figure 20 | Current and voltage in a terminated 50 Ω system

Together with the 50 Ω line (Z0), the internal resistance Ri of the pulse source forms a voltage divider with the pulse voltage V_f and the forward current If at the delay time t_{Delay}. After the delay time t_{Delay}, the pulse hits the load impedance Z_L, in which the pulse is reflected with the voltage Vr and the reflection current I_r. The load current is $I_L = I_f - I_r$. With the leading current I_f and the reflected current I_r, the relationship $(V_f + V_r)/Z_L = (V_f - V_r)/Z_0$ results in the reflection factor

$$r = \frac{V_r}{V_f} = \frac{Z_L - Z_0}{Z_L + Z_0}$$

and thus

$$Z_L = Z_0 \frac{1 + r}{1 - r}$$

For a terminated line with $Z_L = 50\ \Omega$, the reflection r = 0. For a short circuit and open line with $Z_L = 0\ \Omega$ and $Z_L = \infty\ \Omega$, the reflection factor is calculated as r = −1 and r = 1. The voltage at node 1 corresponds to the voltage curve displayed in the oscilloscope of the measuring system. V2 represents the voltage at the load resistor. It is time-dependent on the transit time of the line and corresponds to the voltage after the transit time 2 x t-delay $V_f + Vr = V_f (1 + r)$.

For the TDR analysis of an ESD diode (DUT), the DUT is mounted on a test circuit board. Figure 21 shows the basic measurement set-up. Like the terminating resistor Z_L, the lines have an impedance of 50 Ω. If these are ideal and therefore reflection-free, only the reflection r caused by the DUT and therefore the impedance Z_{DUT} of the DUT is measured.

$$Z_{DUT} = Z_0 \frac{1 + r}{1 - r}$$

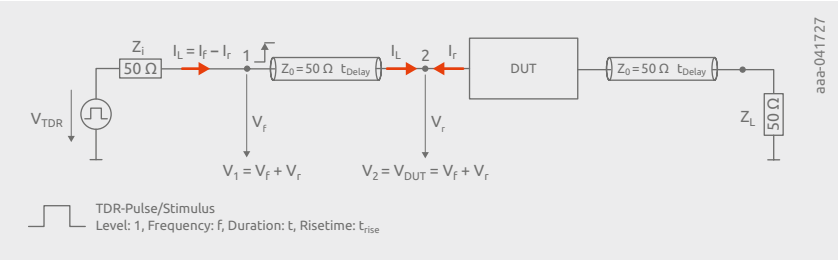

Figure 21 | Current and voltage in a terminated 50 Ω system with DUT

For the measurement, the device under test (DUT) soldered onto a test PCB is connected to the measuring system via a coaxial cable and terminated at the output with 50 Ω to GND. The jump, also known as discontinuity, is evaluated in comparison to an unassembled PCB, shown as an example in Figure 22 for ESD diodes with an SOD962 package.

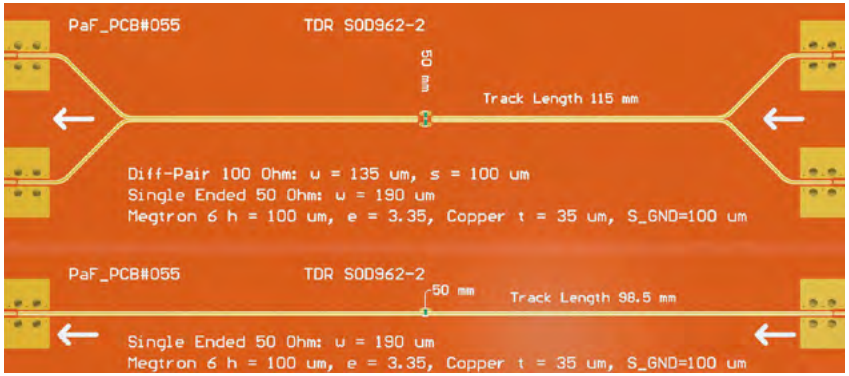

Figure 22 | Test board for differential (100 Ω) and co-planar (50 Ω) TDR measurements

Figure 23a and Figure 23b show the behavior of an ESD diode with C = 160 fF, which is applied to differential lines with 100 Ω impedance and to a coplanar line with 50 Ω impedance and Figure 24 the impedance curve of a single ESD diode on a 50 Ω coplanar line.

Measurement conditions:

- stimulus with frequency 200 kHz and 250 mV
- 250 mV step
- rise time t_{rise} = 40 ps at the DUT
- rise time t_{rise} = 200 ps according to HDMI specification
- measurement of an unpopulated PCB as a reference
- measurement of a PCB applied with ESD diodes.

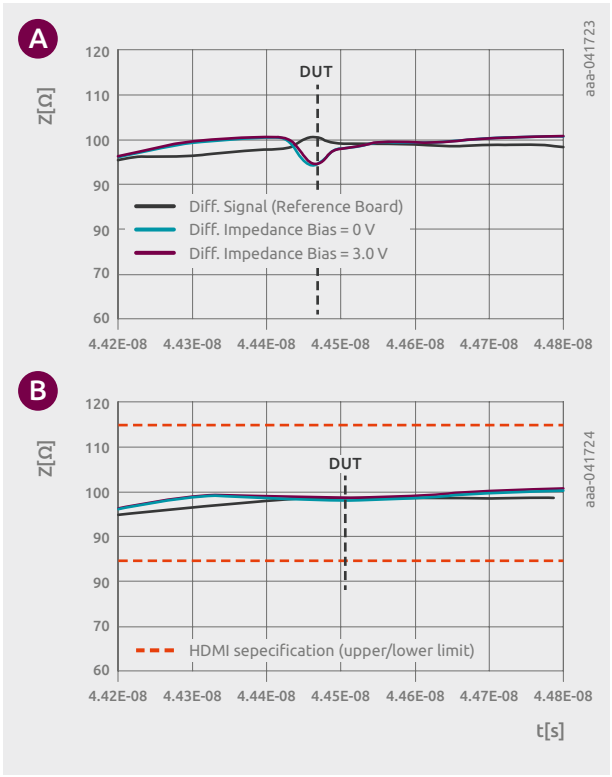

Figure 23 A and B | Impedance curve of an ESD diode on a differential line pair with Z_0 = 100 Ω, measured with t_{rise} = 40 ps and t_{rise} = 200 ps compared to reference.

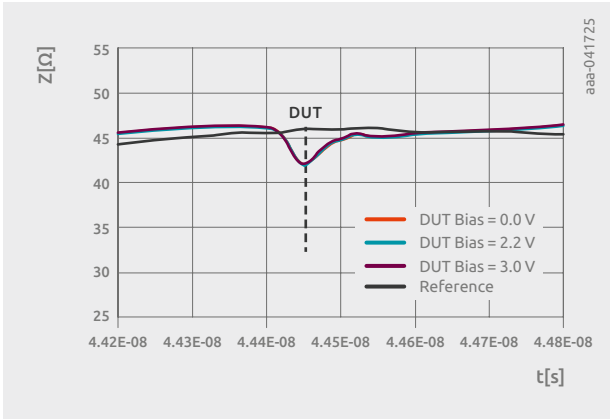

Figure 24 | Impedance curve of an ESD diode with C = 160 fF on a 50 Ω coplanar line in comparison to reference.

Table 3 compares the most important standards. These include the bit time, also known as unit interval (UI), and the rise time t_{rise} [10% … 90%], which is calculated from

$$t_{rise} \approx \frac{0.35}{f_{3\,dB}}$$

The 3 dB cut-off frequency is the fundamental frequency of the respective interface with a bit sequence of 0101. At very high data rates, the actual rise time deviates from the calculated value and is in the range of 30% to 40% of the bit time. To illustrate this, Table 3 shows the line length covered on a data line during the rising edge of the stimulus on the data line when using the PCB material FR4 [ε_r = 4.2].

Table 3: Typical values of high-speed data standards

Interface	Data rate	Bit time	f_{t1}	$f_{t5} = f_{3\,dB}$	t_{rise}	Edge length
USB 1.0	12 MB/s	83.3 ns	6 MHz	30 MHz	11.7 ns	1.71 m
USB 2.0	480 MB/s	2.08 ns	240 MHz	1.2 GHz	291.7 ps	4.3 cm
HDMI 1.4b	3.4 GB/s	2.94 ns	1.7 GHz	8.5 GHz	41.2 ps	6.02 mm
USB 3.2 Gen 1x1	5 GB/s	200 ps	2.5 GHz	12.5 GHz	28 ps	4.1 mm
USB 3.2 Gen 2x1	10 GB/s	100 ps	5 GHz	25 GHz	14 ps	2.05 mm
USB 3.2 Gen 2x2	20 GB/s	50 ps	10 GHz	50 GHz	7 ps	1.02 mm
HDMI 2.1 (FRL)	12 GB/s	83.3 ps	6 GHz	30 GHz	11.7 ps	1.7 mm
USB 4v1	40 GB/s	50 ps	10 GHz	50 GHz	7 ps	1.02 mm
USB 4v2	80 GB/s	39.06 ps	12.8 GHz	64 GHz	5.5 ps	0.8 mm

6.5 Compliance testing

The data interface shown in Figure 25 for transmitting signals at high data rates has a bi-directional design. The losses occurring along the entire transmission path are compensated for by signal pre-emphasis with a feed-forward equalizer (FFE) in the transmitter and a cable equalizer (e.g. a continuous time linear equalizer, or CTLE) in the receiver.

Before establishing data communication via a data interface, the interface's transmission capacity is determined by link training, in which predefined test patterns are sent by the transmitter and compared with the test patterns stored in the receiver. If the test patterns are not identical, the data connection is corrected by comparing the FFE and CTLE using specified table values until data can be transmitted at the maximum data rate. If bit errors cannot be corrected, the interface switches to the next lower data rate and performs a new link training process.

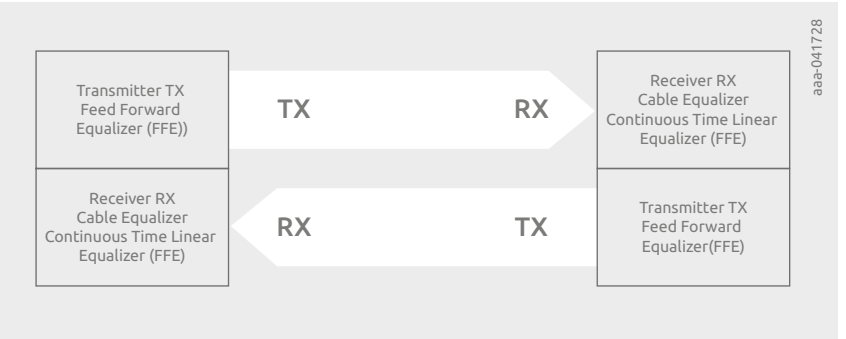

Figure 25 | Bi-directional data interface with transmitter TX and receiver RX

6.5.1 Conformity check of the data interface

An ESD protection diode in a data interface is only a small component of this data interface alongside impedance-controlled lines, vias, coupling capacitors, connectors and cables. To maintain signal integrity, the influence of the ESD diode must be minimal due to its parasitic properties. Therefore, when selecting an ESD diode, the maximum data rate, the rise and fall times of the data signal and the resulting bandwidth should all be considered. The S-parameters and a TDR test of the ESD diode provide an initial indication of the suitability of the ESD diode in the interface.

The conformity test is a complete system test for the protocol and physical layer. It provides a precise statement about the functionality and robustness of the interface and must be carried out for each application of the interface to ensure the interoperability of the data interface.

6.5.2 Physical layer test

One component of the conformance test is the measurement of the physical layer of the data interface. To assess the signal quality of a data stream, an eye diagram is generated by superimposing the bits of a randomly sampled data stream. This makes it possible to analyze extreme bit sequences with a maximum data rate of 101010 and more static bit sequences with 100000 or 011111. The representation of an eye diagram is related to the bit time (unit interval (UI)). The parameters in the list below are measured and analyzed:

- eye amplitude
- crossing point
- lowest and highest level
- rise and fall time
- total jitter
- temporal change of the zero crossing
- eye height
- eye width
- bit time (unit interval (UI)).

The mask consists of an inner mask and an upper and lower mask. Overshoots and undershoots, jitter or reflections must not violate the mask elements. The mask is a hard condition and therefore a clear pass/fail criterion. Figure 26 and Figure 27 show the TX mask and the measured values of an eye diagram.

The JEDEC standard JESD8-18A describes the compliance test of the physical layer of the data interface in detail.

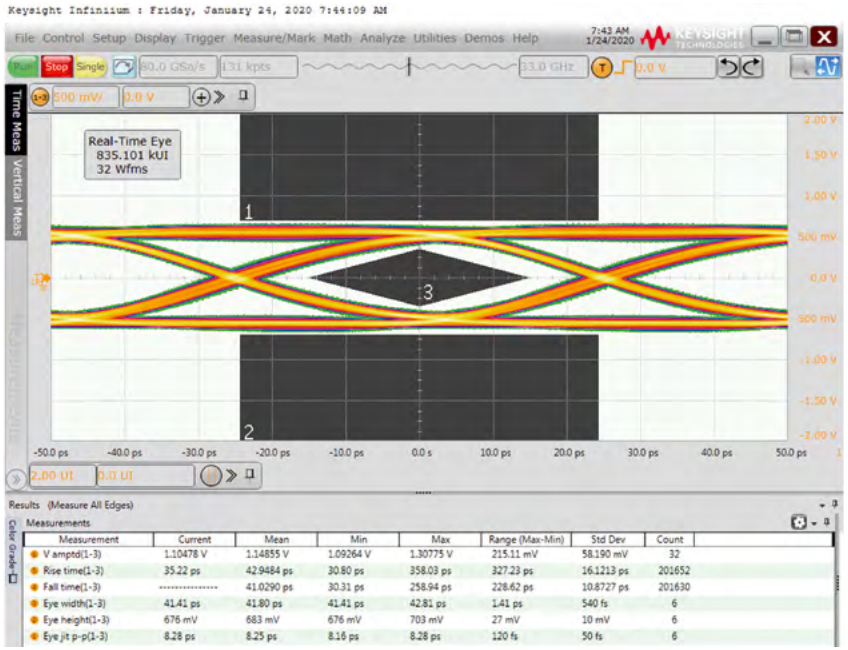

Figure 26 | Eye diagram of a transmitter with mask

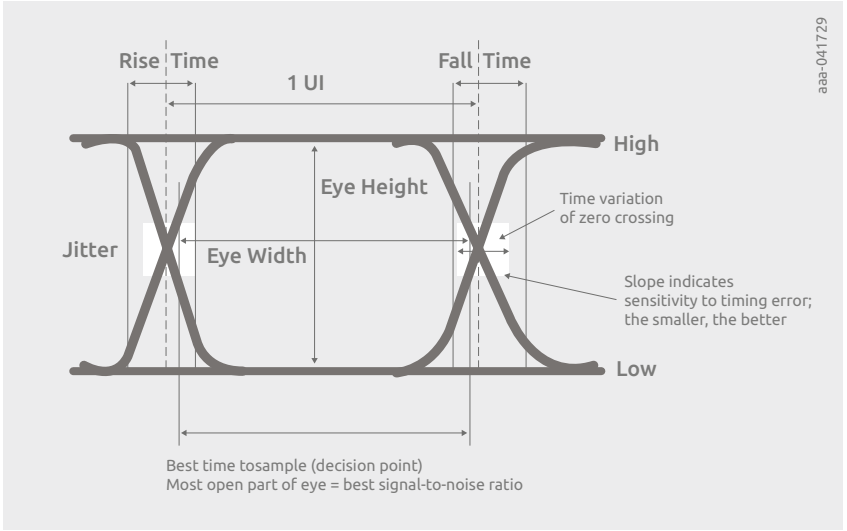

Figure 27 | Eye diagram with typical characteristics for assessing quality

6.5.3 HDMI 2.1

As the topology of the various interfaces and the test procedures are similar, only HDMI 2.1 is considered. The physical layer shown in Figure 28 consists of:

- a transmitter (source)
- connectors
- cables
- a receiver (sink) with cable equalizer.

The cable is described by S-parameters as short cable model (SCM) and worst cable model (WCM).

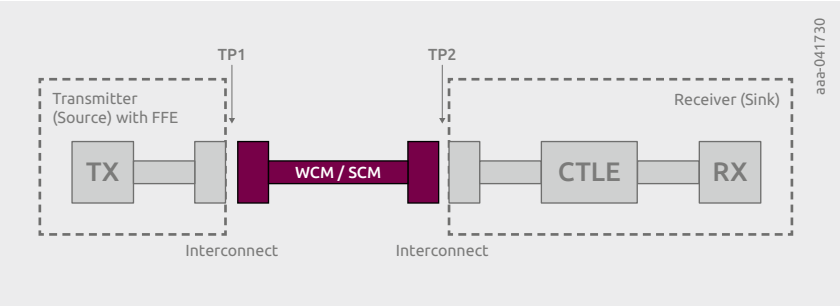

Figure 28 | TMDS and FRL link test points

The tests differ in:

- **Transmitter test at test point 1 (TP1)**
  Evaluation of the output signals of a graphics card or a set-top box with an oscilloscope. The transmitter has signal pre-processing using a feed-forward equalizer (FFE). The FFE is not used when testing the ESD diodes.
- **Testing the receiver at test point 2 (TP2)**
  Evaluation of the sensitivity of a video output device with specified test patterns of the pattern generator, WCM and reference cable equalizer, implemented as CTLE. The equalizer has an adjustment range of 1 dB to 8 dB to compensate for losses on the transmission path. In addition to a statement about the functionality, the test also provides a statement about the sensitivity and robustness of the receiver to be tested. To test the ESD diodes, the eye diagram and the eye opening are determined using the FRL receiver mask shown in Figure 29.

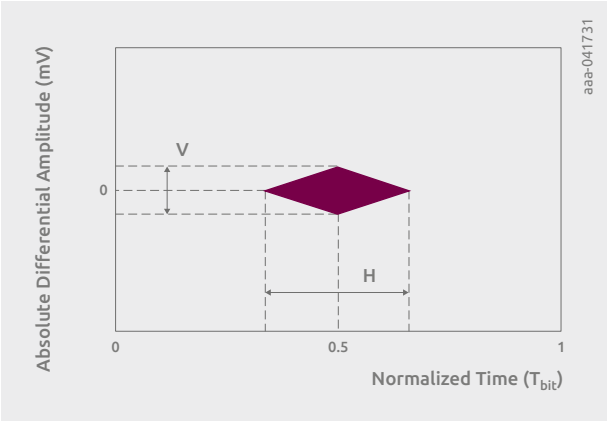

Figure 29 | FRL receiver mask

6.5.4 Testing ESD diodes

Due to the complexity and the different possible uses of the interface in the end product, it is not possible to precisely determine the influence a single ESD diode will have on the data link. For this reason, the test is significantly reduced and the ESD diodes are set up on a test circuit board, as shown in Figure 30, on differential lines with an impedance of 100 Ω.

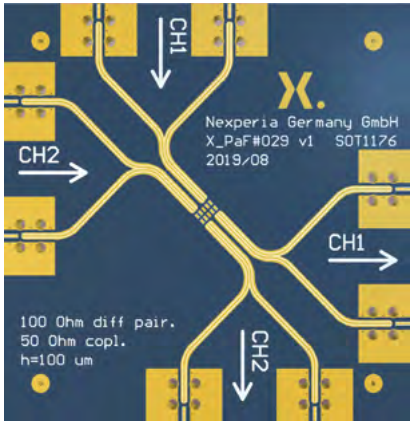

Figure 30 | Test circuit board for SOT1176 (DFN2510A-10) packages

For the measurements, the circuit board is connected to a pattern generator, in this case an arbitrary waveform generator, with implemented S-parameters of the WCM, as shown in Figure 31. The output side of the PCB is connected to a serial data analyzer with an integrated continuous time linear equalizer (CTLE) as a reference cable equalizer. The data signal is measured at TP2 as an eye diagram.

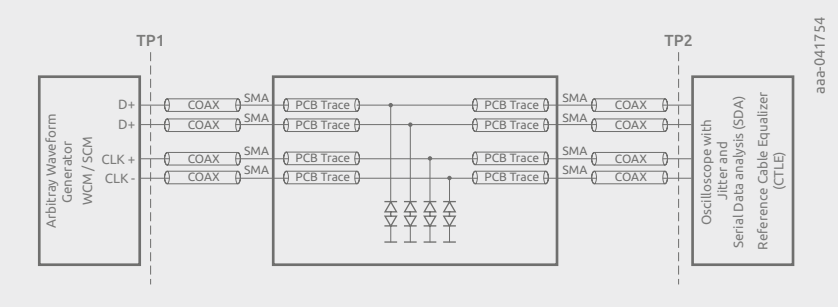

Figure 31 | Test set-up of the HDMI link with test circuit board

For the analysis, an unpopulated reference PCB is measured in comparison to a PCB with the ESD diodes under investigation at the maximum data rate of 12 GB/s for FRL. The equalizer is adjusted down from the maximum eye opening of 8 dB to the first violation of the inner FRL receiver mask. Figure 32 and Figure 33 show a comparison of the eye diagrams for an unpopulated reference PCB and a populated PCB with ESD diodes at equalizer settings of 5 dB and 6 dB.

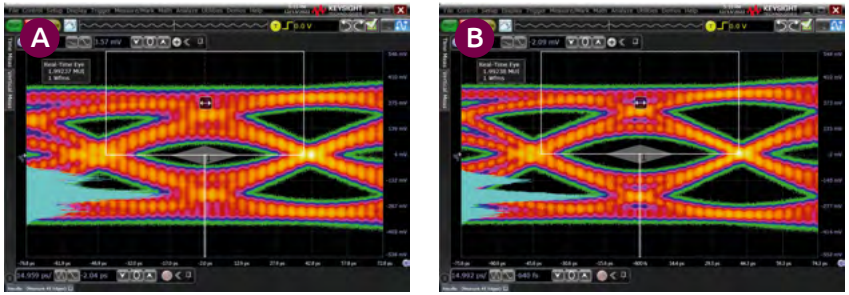

Figure 32 A and B | Receiver mask test of a reference PCB at 5 dB and 6 dB

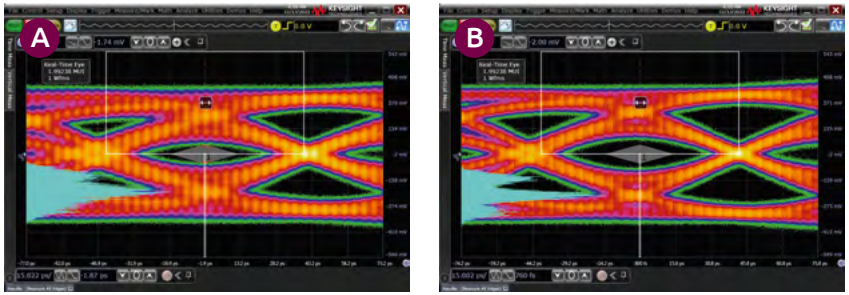

Figure 33 A and B | Receiver mask test of a PCB with ESD diodes at 5 dB and 6 dB

6.5.5 Simulation of the HDMI 2.1 link with ESD diode

In addition to metrological analysis of a fast data interface, simulation makes it possible to evaluate the data connection's functionality.

For this purpose, the measurement set-up must be fully described in a simulation environment and adapted to the standard to be examined, as shown in Figure 34. The necessary transmitter, receiver and cable components are predefined in libraries and are extended by the specified values. The DUT shown in Figure 35, which contains the coaxial cable, the test board and the ESD diodes, is modeled with S-parameters. The WCM and SCM cable models required for the receiver test are used as predefined scattering parameters in the simulation.

Control is via Source with the settings:

- signal amplitude 1 Vpp in a 50 Ω system
- data rate 12 GB/s
- rise and fall time 30 ps.

The FRL receiver mask and the CTLE data defined in the specification are implemented for evaluation in the receiver. The simulation then takes place in steps of 1 to 8 dB of the CTLE and generates a separate eye diagram for each step.

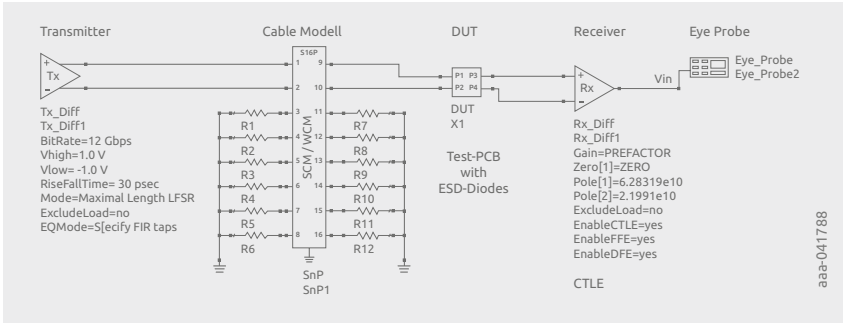

Figure 34 | Simulation model of an HDMI 2.1 receiver interface

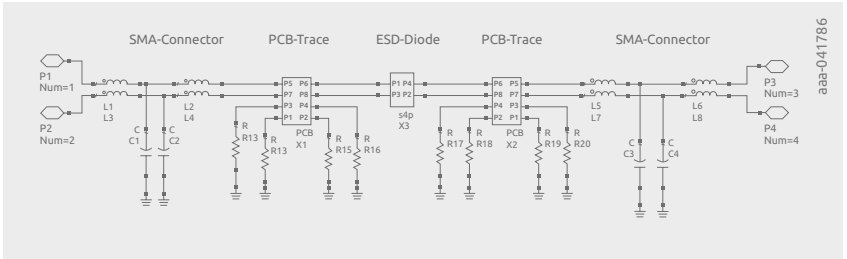

Figure 35 | DUT-modeled elements of the test circuit board with ESD diode

6.5.6 Simulation results

For a direct comparison between simulation and measurement, the scattering parameters of the measured device were integrated into the simulation. The eye diagrams in Figures 36 A & B show the results of the receiver mask test for the equalizer values of 5 dB and 6 dB determined during the measurement. Similarly, Figures 37 A & B show the simulated eye diagrams of the unassembled reference PCB at 5 dB and 6 dB.

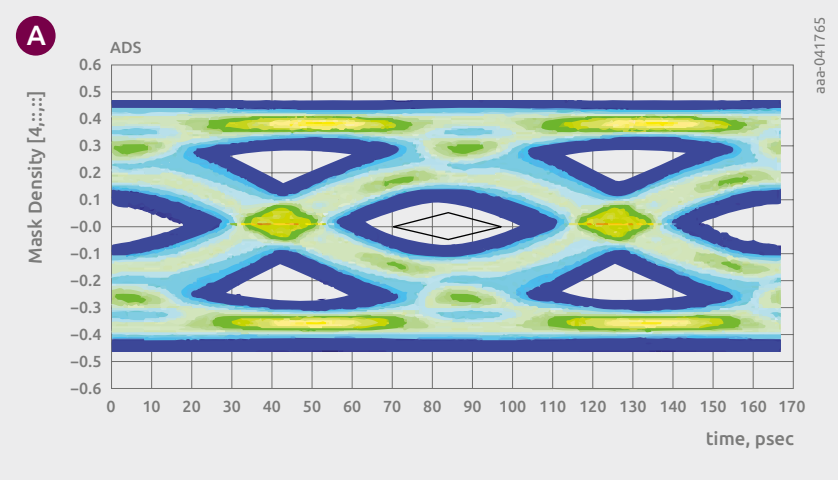

Figure 36 A and B | Simulated receiver mask test of a reference PCB at 5 dB and 6 dB

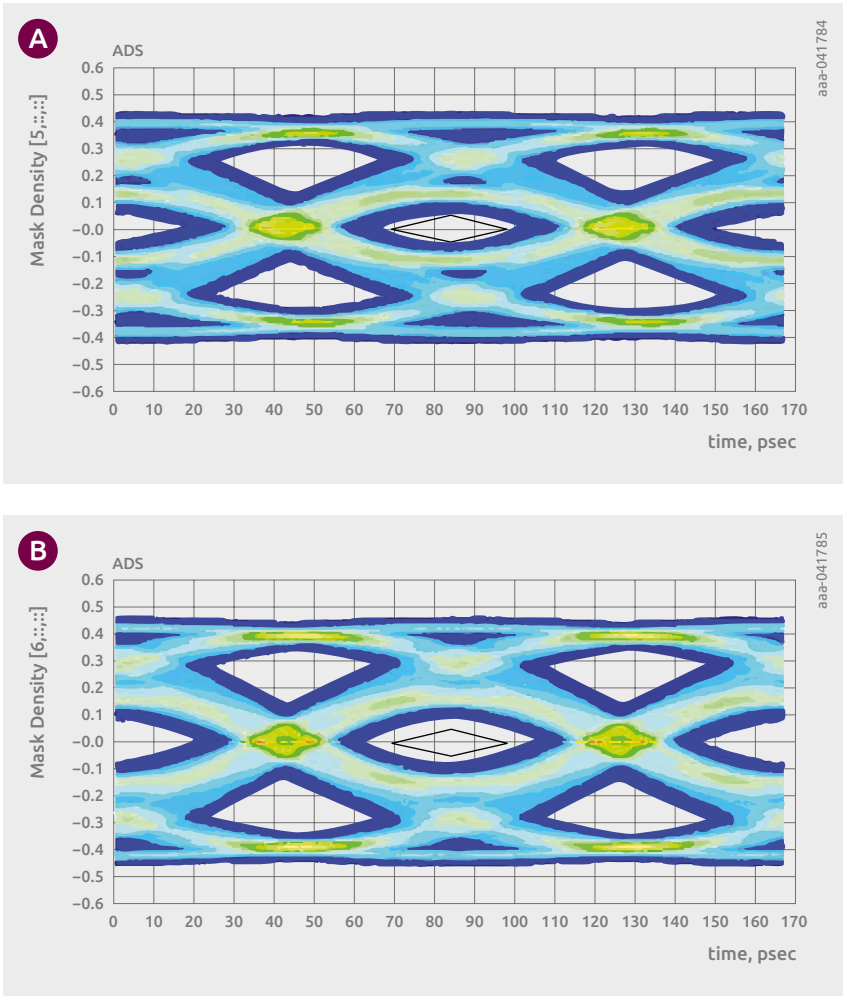

Figure 37 A and B | Simulated receiver mask test of a PCB with ESD diodes at 5 dB and 6 dB

The comparison between simulation and measurement shows that the simulation results of the receiver's mask test approximate the measurement results well.

6.6 Layout and routing of ESD protection devices to optimize signal integrity

Maintaining signal integrity (SI) is the key objective for high-speed interface designs across all industries. Signal integrity is usually a standard requirement on the entire link or channel including the PHYs, PCB, cable and connectors, as shown in Figure 38. The signal sent from the Tx is not allowed to degrade to the extent that quality is diminished too much before reaching the Rx. All components along the signal path can have an impact on the signal, but the main causes of degradation are usually the cable and connector. Most high-speed cables are shielded and are developed based on rigorous quality standards. However, all cable materials have their physical limitations. Insulators, for example, are lossy and linear in length and frequency. This means that with increasing length and higher data rates, design engineers need to deal with these signal losses. Also, connectors create a bottleneck. In mobile applications, for example, USB-C connectors can be surface-mounted devices (SMDs) which increases the potential to pass the SI requirements. In automotive, additional efforts are needed to support the longevity of a car in terms of being more robust against vibration and shock, so most of the connectors are through-hole types which pose an additional challenge for SI. Usually, cables and connectors are the elements that have the biggest impact on SI. However, ESD protection can significantly degrade the signal when the wrong choices are made in terms of device capacitance or package (or both). The routing to and from the ESD device can also make the difference, especially in upper GHz range.

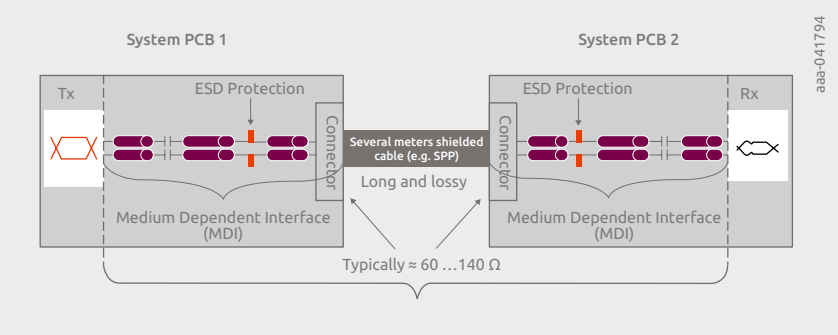

Figure 38 | Signal integrity challenges for designs considering all components of a typical high-speed interface

The part of the SI which is related to the ESD protection device can be separated into three portions:

- Device capacitance C_d: This parameter is a simplified equivalent circuit for the ESD device but very useful to judge the SI capabilities. In most cases, this parameter is also the dominant one for SI behavior, because for each interface there are recommendations given for its value (see Figure 39). For increasing data rates, requirements for C_d are becoming stricter which results in a very low C_d far below 1 pF for high-speed interfaces such as SerDes and USB.

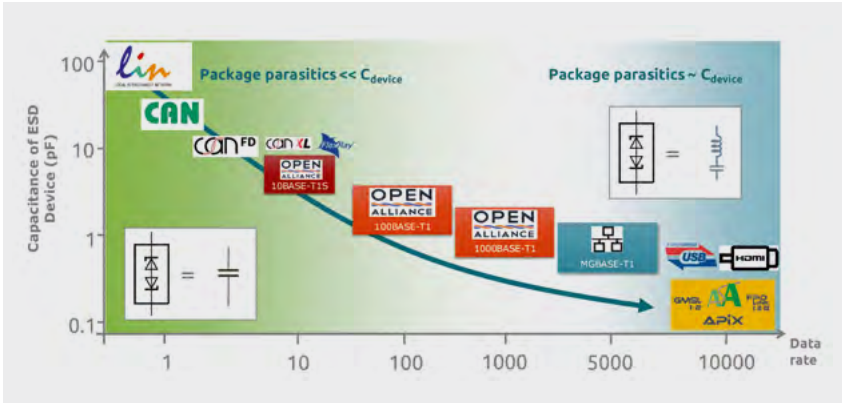

Figure 39 | Device capacitance against the data rate for the most popular interfaces

- With increasing data-rate and low C_d values the package and its parasitics become increasingly dominant and compact packages with reduced parasitics are required.
- Also, the routing from and to the ESD device and adjacent PCB layout can make a difference. This is related to the package because the pin pitch and overall package size can have a significant influence on the local dimensions of the traces and hence on the local impedance of the path.

Once target capacitance has been identified for the target application there is the question of which kind of package should be selected. The higher the data rate the more the package dominates SI behavior. Figure 40 shows the difference between SOT23 and DFN1110-3 in terms of IL, RL, and MC (mode conversion).

In both packages a silicon diode with 5.2 pF capacitance is used. It can be seen that the leadless DFN1110-3 clearly outperforms the SOT23 especially in IL by ~400 MHz just because of the significantly larger parasitics of the SOT23.

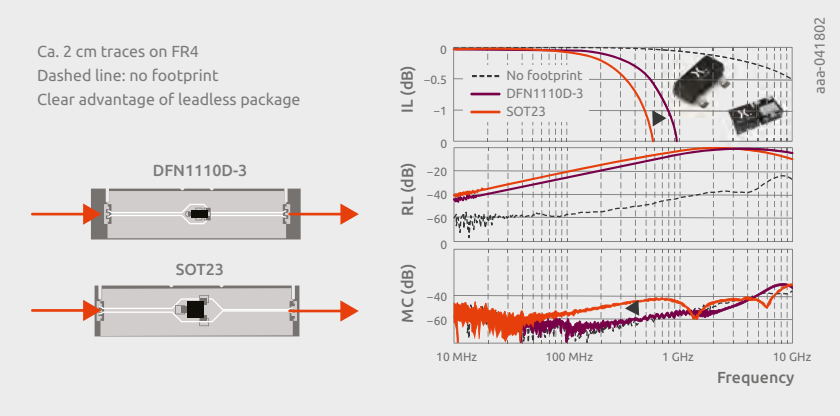

Figure 40 | Leaded and leadless pins compared in terms of S-parameters

The best SI scenario for the PCB part of the MDI (from PHYs pins to the connector pins) is a straight line without any bending or curves for both, single-ended and differential transmission. For a given layer stack-up, the impedance of the data lines can be easily adjusted to the system impedance (typically 50 Ω or 100 Ω for single ended and differential, respectively). Additional components such as CMC, termination networks or ESD protection would not only add a discontinuity to the traces but also change the impedance of the traces due to the package size, pin configuration and pin pitch.

For single-ended traces, two-pin devices are usually used. The best way to ensure signal integrity (and for ESD) is to route the trace over the pad of the device avoiding stubs (see Figure 41).

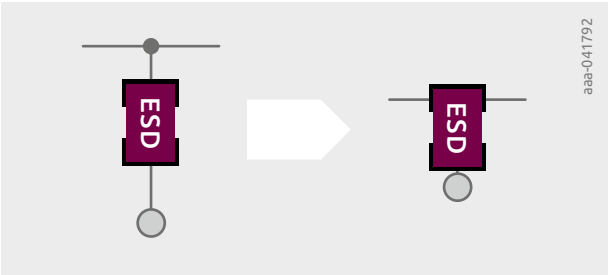

Figure 41 | Avoiding stubs improves SI

The routing should always be over the pad for both SI and ESD purposes. Also, the GND connection (typically using a via) should be positioned close to the ESD device (see Figure 42).

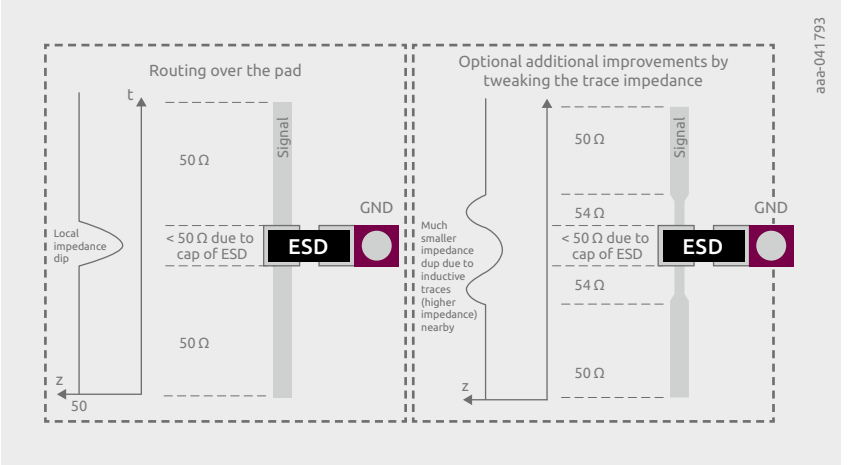

Figure 42 | Routing of two-pin ESD protection devices for single-ended traces. The routing should be done over the pad with a solid GND connection close by (left). Further improvements by narrowing the traces locally to increase the trace impedance to compensate for the impedance drop caused by the capacitance of the ESD device (right).

In this case the capacitance would still create an impedance drop and the compliance of the SI would be strongly dependent on the capacitance value. In most cases, the high-speed designer would choose an ESD device with low enough C_d value to meet all SI requirements. However, in some cases this might not be sufficient and additional measurements should be performed. One option is to tweak the impedance of the trace locally to slightly increase its impedance and compensate for the capacitance drop caused by the ESD device, as reported in [1]. The right-hand side of Figure 40 shows an example of this method. It should be noted that in case of tweaking the local trace impedance should be verified for a given ESD device in terms of the value of the impedance increase and length of the trace.

For differential transmissions, two-pin and multi-pin packages can be used. For two-pin packages the best routing is directly over the pad (see Figure 41). To maintain the differential impedance the routing of the traces should not be parallel. However, the capacitance of the ESD diode might cause local impedance dip. If this dip exceeds tolerance (typically ±10% of the reference impedance) it needs to be compensated. This can be achieved by GND cutout, as shown in Figure 44. Details of this approach will be described in a parallel publication due to appear in an IEEE publication in Q4 2024 (issue to be confirmed).

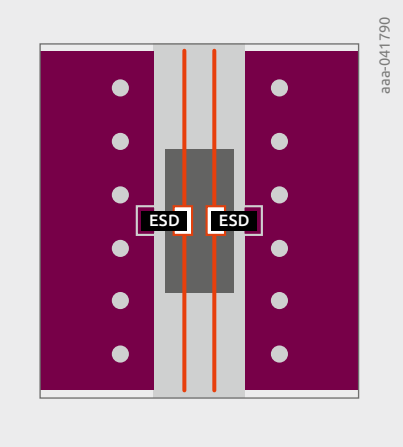

Figure 43 | Routing of a two-pin ESD device on differential lines

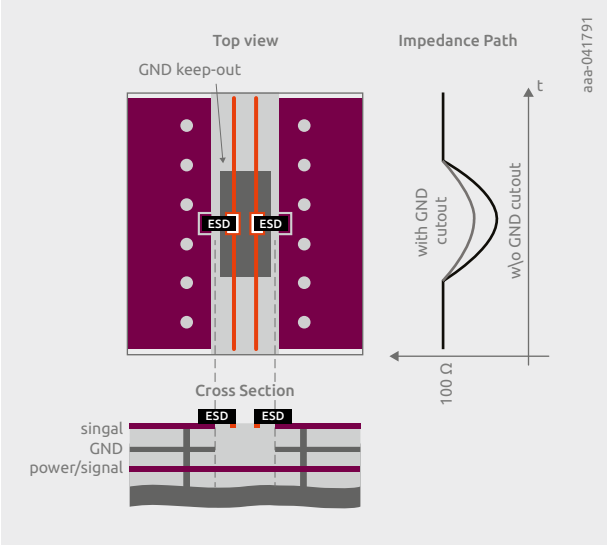

Figure 44 | Differential routing with GND cut-out to compensate for the impedance dip caused by the capacitive of the ESD device. On the right the compensation is illustrated using TDR

For three-pin devices such as DFN1006LD-3 there are in general two routing options (see also Figure 45A).

1. Through routing, where the spacing of the differential lines is chosen according to the pitch of the ESD package so that the impedance of the differential pair is not impacted by the ESD protection device. This is only possible for a different stack-up/prepreg configuration since the impedance is strongly dependent on them (V1_1/2 in Figure 45A).
2. The spacing of the differential lines is smaller than the pitch and the package and the spacing needs to be adapted slightly.

From the comparison terms of differential IL (see Figure 45B) we see a slightly better performance with the second option. The widening of the differential pairs increases the impedance of the traces slightly, but the capacitance of the ESD diode partially, which results in a better performance.

In both versions, the placement of the GND via (on one or other side of the ESD device) does not play any significant role, which provides the designer with more flexibility.

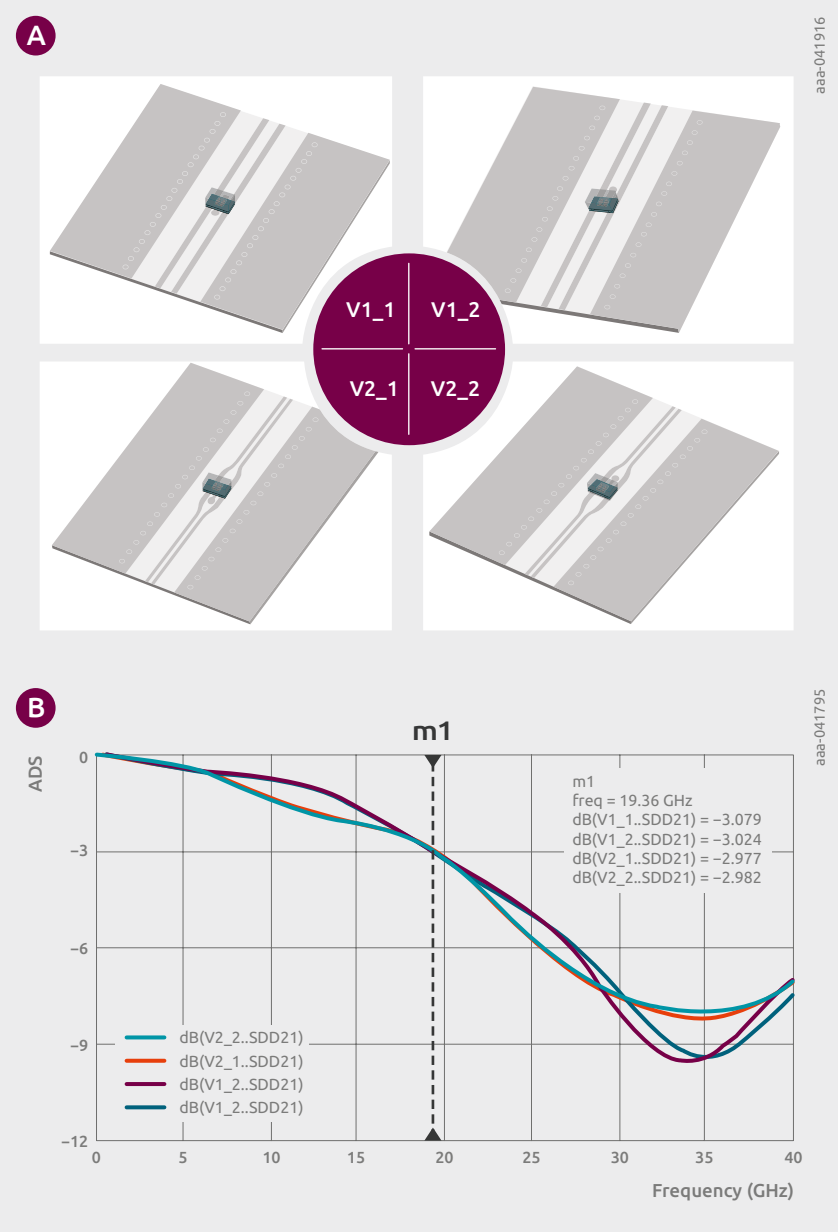

Figure 45 | Routing options for the tree-pin DFN1006LD-3 (A) and the performance of in terms of differential IL

Other packages such as SOT23 are often used for interfaces with lower data rates, such as LIN, CANFD, and automotive Ethernet up to 1000Base-T1. It is useful to know about the optimal routing options for this, which are shown in Figure 46.

Even if the winding of the traces due to the pitch increases the impedance of the trace, as in case A, the compensation by the diode's capacitance is significant and helps to improve the S-parameters as shown in Figure 47. Also, the symmetry of the package might be particularly important since it shows lowest mode conversion.

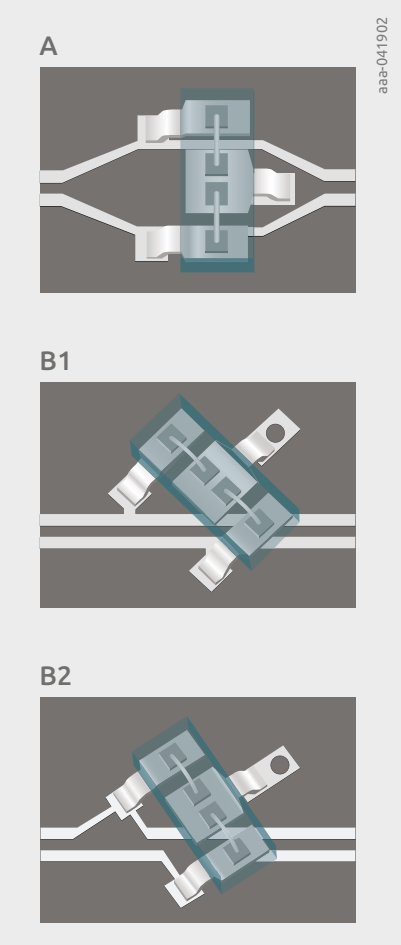

Figure 46 | Routing options for the SOT23 analyzed by a full 3D model using CST MW Studio [2]

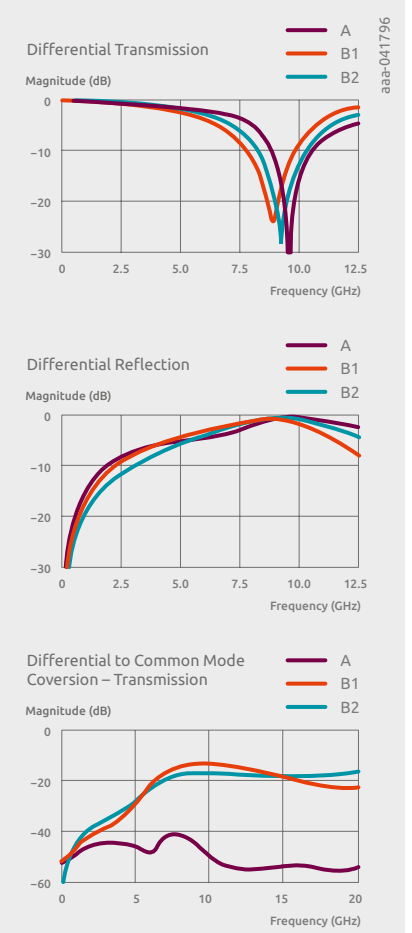

Figure 47 | S-parameters for the case study shown in Figure 46

It should be mentioned that the routing from and to the ESD protection device can significantly improve the interface's overall SI performance. However, for interfaces with low or medium data rate in the lower GHz range, the capacitance of the ESD device and the package parasitics might be more dominant. In those scenarios where the capacitance is extremely low anyhow and where the package parasitics are extremely small as well, an optimum layout design can become the key factor for good signal integrity.

References

[1] M. Pilaski, A. Hardock, "InCompliance," https://incompliancemag.com/local-pcb-layout-tweaks-for-improved-signal-integrity-when-using-esd-protection-devices/

[2] D. Systems, Dassault Systems, https://www.3ds.com/de/produkte-und-services/simulia/produkte/cst-studio-suite/

Chapter 7

Interfaces and applications

7.1 USB standards, data speeds and coding methods

7.1.1 USB 1.0 and USB 2.0 interfaces

Table 1 shows an overview of contemporary USB standards and their related symbol rates.

Table 1: Overview of data rates for USB interfaces

USB Type	Speed class	Data Rate	Symbol rate (Baud rate) Coding method
USB 1.0	Low Speed (LS)	1.5 Mbit/s = 187.5 kByte/s	1.5 MByte/s NRZI-Code with Bit-Stuffing
USB 1.0	Full Speed (FS)	12 Mbit/s = 1.5 Mbit/s	12 Mbit/s NRZI-Code with Bit-Stuffing
USB 2.0	High Speed (HS)	480 Mbit/s = 60 MByte/s	480 Mbit/s NRZI-Code with Bit-Stuffing
USB 3.0	Super Speed	4000 Mbit/s = 500 MByte/s	5000 Mbit/s 8b10b-Code
USB 3.1	Super Speed +	9697 Mbit/s = 1212 MByte/s	10000 Mbit/s 128b132b-Code
USB 3.2	Super Speed +	2 lane operation with Type-C connector operation; doubling of effective data rate	

USB 1.0 and USB 2.0 use non-return-to-zero-inverted (NRZI) coding, also known as NRZ coding. Typically, this follows a simple rule:

state 0: toggle | state 1: constant

When this method is applied, the polarity of a connecting wire pair in a cable has no impact on the bit sequence. This is an advantage because a change in polarity represents a 0 state, regardless of direction of transition. Figure 1 shows the schematic of the logic required for the hardware implementation of an NRZI encoder. The input signal is fed to an inverted input of an Exclusive-Or (XOR) gate, a digital logic gate that gives a true (1 or high-state) output whenever exactly one of the inputs has a 1-state. If both inputs are 1, or both are 0, the output equals false (0 or low-state).

Behind the XOR gate, a flip-flop samples the output of the gate by the system clock. The output of the flip-flop represents the output of the coder and feeds back into the XOR gate as the second input signal for this gate.

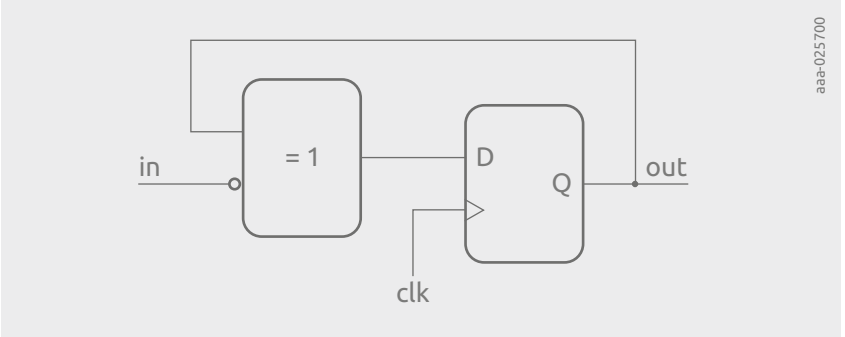

Figure 1 | NRZI(S) encoder circuit

In Table 2 an exemplary bit stream is encoded by the NRZI coder. The second row shows the inverted input bit stream, the third row the output of the XOR, and the fourth row the coded output signal. The output bit stream shows the desired logic of a polarity toggle, which is created by a logical 0 in the input stream, with no change in the output stage for a logical 1 in the input data stream.

Table 2: Example of NRZI(S) encoding

input	1	0	0	0	1	1	1	0	1	0	1	1	0
inverted input	0	1	1	1	0	0	0	1	0	1	0	0	1
output XOR	0	1	0	1	1	1	1	0	0	1	1	1	0
Encoder output	0	0	1	0	1	1	1	1	0	0	1	1	1

Figure 2 shows a simplified schematic of a decoder for an NRZI data stream, which detects a signal change with an output as logical state 0 and no signal change as logical state 1.

The function is realized by an XOR gate, where the data stream is connected to one input and the second input is connected to the output of a flip flop which provides the prior state of the encoder. Finally, the output of the XOR is inverted to derive the correct polarity.

Table 3 illustrates how the decoder works, showing the bit stream at the input in the first row, the output of the flip-flop, the output of the XOR gate before the inversion, and the final output of the decoder in the last row. The output stream of the decoding stage is identical with the input stream of Table 2.

Note that in signal transmission it is preferable to have a DC-free system. Consequently, it is not necessary to have a direct galvanic connection for cable transmission between transmitter and receiver. The frequency band of the data channel does not need to start at 0 Hz but can be designed to have a higher value. This ensures that data transmission can operate within a smaller frequency band.

Whenever a 0-state is transmitted, NRZI coding ensures that changes are incurred on the data during transmission. A constant high can cause the signal to become stuck, with no oscillations occurring. For this reason, a signal change has to be forced after 6 bits in high-state, which is applicable to all USB standards. Note also that seven subsequent high-states indicate a bit sequence error.

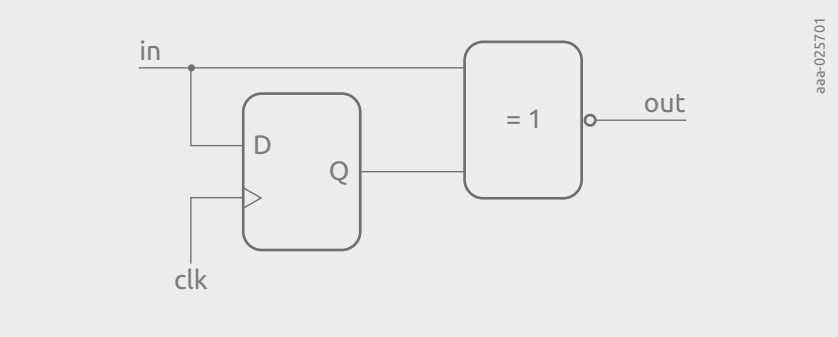

Figure 2 | Decoder schematics

Table 3: Example for NRZ decoding

input to decoder	0	0	1	0	1	1	1	1	0	0	1	1	1
output of flip-flop	x	0	0	1	0	1	1	1	1	0	0	1	1
output XOR	x	0	1	1	1	0	0	0	1	0	1	0	0
output decoder	x	1	0	0	0	1	1	1	0	1	0	1	1

Whenever a D+ signal is in low-state and D– is in high-state, the USB bus data line state is described as K-state. J-state describes the opposite condition, where D+ is in high-state and D– low-state. Whenever both signal lines are pulled low, the system is in single-ended zero condition, referred to as SE0.

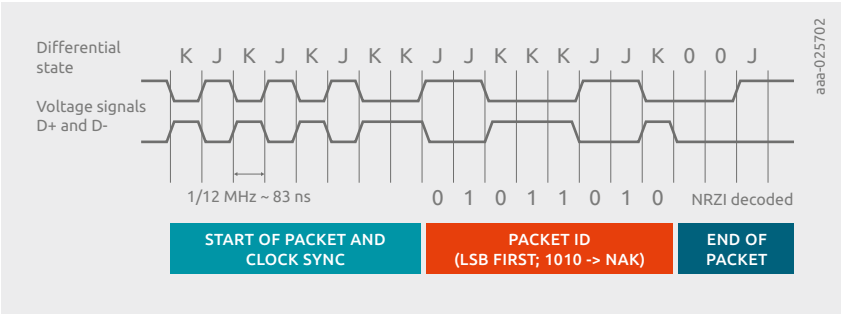

Figure 3 | Example of a data stream on a USB 1.1 full-speed interface

Figure 3 shows the example of a brief data stream transmitting a NAK (Not AcKnowledged) packet at a bit rate of 12 Mbit/s, via USB 1.1 at full speed. NAK indicates that data cannot be read out (for example, because of problems with the receiving and/or sending device/s).

Whenever real data content is transmitted, data packets are placed between the packet ID and the end-of-packet (EOP) block. The last packet of the sequence is implemented with two SE0 states, followed by one idle J-state. Data transmission begins with an idle J-state: a 00000001 sequence, i.e. a KJKJKJKK sequence.

In USB 2.0 high-speed mode, the start sequence is 32 bits long. This provides more transitions, enabling the clock recovery phase-locked loop (PLL) circuit to synchronize in exact correspondence to the timing of the bit stream.

When no device is connected, the host pulls other signal lines to ground via a 15 kΩ pull-down resistor. If a USB device is connected, one of the signal lines is pulled high via a 1.5 kΩ resistor and overwrites the pull-down state of the host.

USB 1.x speed is determined whenever a D+ or D– line is pulled high via the 1.5 kΩ USB pull-up resistor. J-state signifies the idle state for USB full-speed mode;

K-state signifies low-speed. A reset to SE0 condition occurs when both signal lines are pulled low by the host for 10 to 20 ms. If a USB 2.0-ready device is connected, the above procedure for USB 1.1 devices is performed initially, but continues with another process.

After reset, the device puts a K-state on the bus telling the host that it can handle the higher speed. After this the host toggles three times between J and K state to tell the USB device that the host can also support the high-speed data rate. This handshaking procedure for the speed capability of host and device is known as 'chirping'.

7.1.2 USB 2.0 eye diagrams

The USB standard specification defines four measurement planes that are used to test a USB interface, as depicted in Figure 4. TP1 connects directly to the signal lines of the transceiver of the hub circuit board. TP2 connects the USB cable. TP3 is located directly at the input connection point of the USB device. TP4 connects directly to the pins of the receiving block of the device circuit board.

In an eye diagram measurement, an oscilloscope shows the bit transitions of a data path as an overlay of many single traces with random data content. Because no separate clock signal is provided on an extra signal line, the oscilloscope is triggered with a recovered bit clock signal. A data clock recovery PLL provides the data sampling clock, synchronized to data transitions.

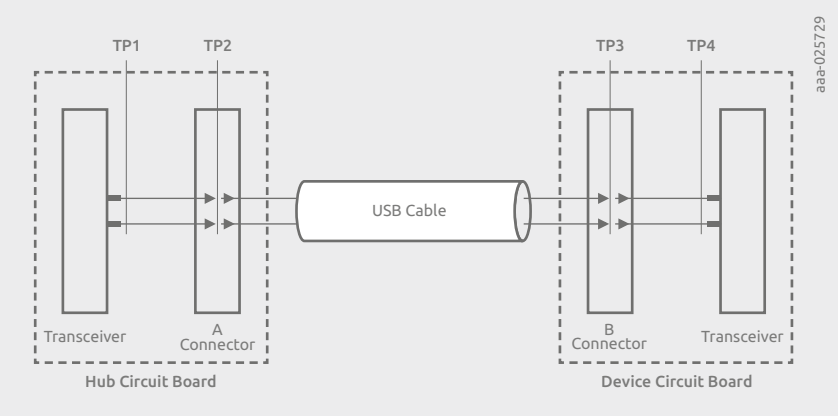

Figure 4 | Measurement planes for eye diagrams

The data eye diagram is a methodology that helps to analyze the signal quality of a high-speed digital signal. Ideally, an eye diagram with a binary signal shows a row of rectangular boxes. However, in real scenarios the rise and fall times are not zero but are extended both by parasitic capacitances in the data path and by the limited speed of the transmitter stages.

Reflections, overlay of noise, and jitter of the PLL clock render a graph with a smaller open temporal window, the part of the eye diagram where no signal transitions occur. Data transitions are not located at exactly n times the symbol length. Jitter can have either a random distribution or a deterministic distribution, depending on its root cause. The nature of the jitter can be analyzed with a histogram. The width of the complete histogram represents the peak-to-peak jitter.

Figure 5 shows how the waveforms of transmitted data for a hub, measured at TP2, or for a device, measured at TP3, should appear. In a standard-compliant scenario, no signal traces are noticeable within the inner mask of the diagram, which is defined by points 1 to 6, as listed in Table 4. Each of these points is defined by a certain voltage and time within the unit interval. The unit interval is equal to the symbol length.

High-speed USB shows:

$$T_{symbol} = 1/f_{symbol} = 1/480\ Mhz = 2.0833\ ns$$

The temporal location is listed as a percentage value of the unit interval in the table. The nominal voltage swing of USB 2.0 is +400 mV to −400 mV. The diagram shows a second mask, which limits the signal in terms of higher voltages. The maximum voltage for the signal is ±475 mV, for a period during which no transitions occur. The voltage limit at transitions is ±525 mV, which allows some room for over- and under-shoots.

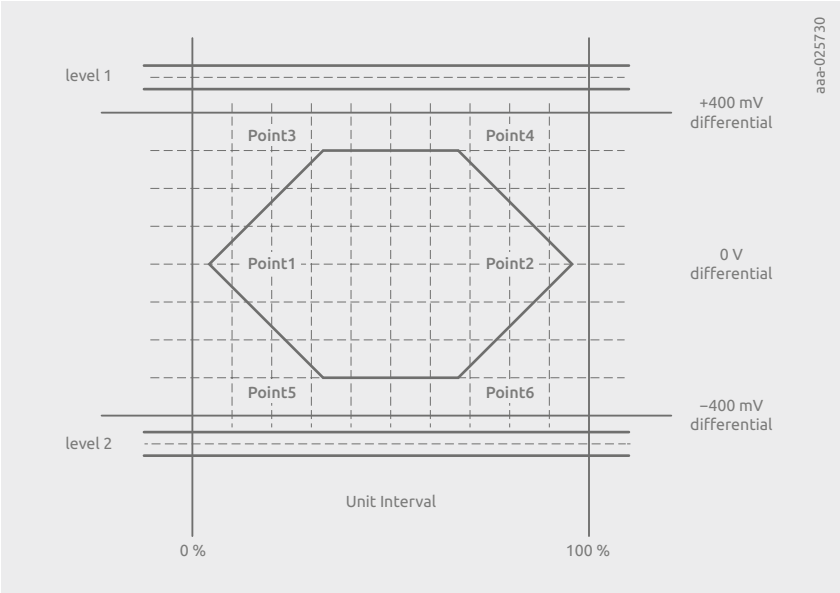

Figure 5 | Transmit waveform requirement for a hub (TP2) or a device (TP3) without a captive cable

Table 4: Parameters for the USB transmitter eye for the test case in Figure 3

	Voltage level (D+, D–)	Time (% of Unit Interval) 1/480 MHz = 2.0833 ns nominal
Level 1	525 mV in UI following a transition, 475 mV in all others	–
Level 2	–525 mV in UI following a transition, –475 mV in all others	–
Point 1	0V	5%
Point 2	0V	95%
Point 3	300 mV	35%
Point 4	300 mV	65%
Point 5	–300 mV	35%
Point 6	–300 mV	65%

Figure 6 shows a receiver waveform requirement scheme for a signal applied to TP4/device transceiver or to TP1/hub transceiver. The receiver mask is typically smaller than the transmitter mask, as stated above. The height of the eye is 300 mV, with a –150 mV to +150 mV range. The width of the eye is reduced to 60% of the unit interval.

Table 5 contains the details for the keep-out area for this particular test condition, which shows the smaller inner mask, as well as the upper and lower boundaries as outside limits for the D+ and D– signal waveforms.

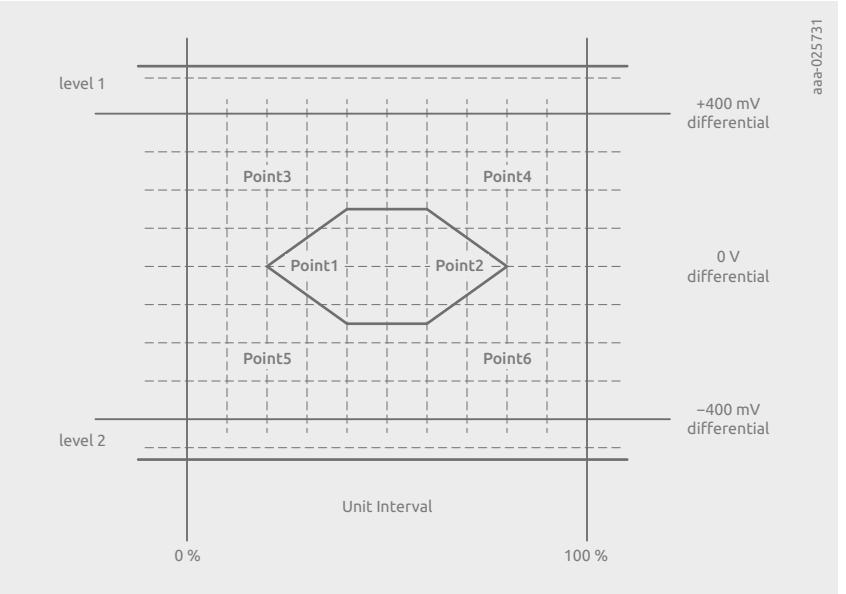

Figure 6 | Receiver waveform requirements for USB 2.0 with a signal applied at TP4 for a device transceiver or a hub transceiver with a signal applied at TP1

Table 5: Parameters for the USB 2.0 receiver eye

	Voltage level (D+, D–)	Time (% of Unit Interval) 1/480 MHz = 2.0833 ns nominal
Level 1	575 mV	–
Level 2	–575 mV	–
Point 1	0 V	20%
Point 2	0 V	80%
Point 3	150 mV	40%
Point 4	150 mV	60%
Point 5	–150 mV	40%
Point 6	–150 mV	60%

7.1.3 USB 3 Gen 1 and Gen 2 interfaces

USB 3 Gen 1 and Gen 2 use a different DC content removal method on signal lines, referred to as 8b/10b encoding, in which 8-bit data is replaced by 10-bit data. Thus, redundancy is added to obtain both a DC-free bit stream and a limited disparity of transmitted 0-states and 1-states. In a row of 20 bits, the counts of the two possible states shall never differ by more than ±2.

Note that after several 8b/10b code words, the signal is completely DC-free and the number of ones and zeros is identical. The 8-bit original data is split into 5 bits, which are coded in 6 bits with a 5b/6b-code. The remaining 3 bits are coded in 4 bits with a 3b/4b-code, creating the final 8b/10b encoding scheme.

The coding operates on a running disparity (RD): after each symbol, the count of ones and zeros differs either by 1 or −1. Table 7 lists the RD coding rules. For clarification, two processes based on the rules in Table 10 are explained:

- If a code word has a disparity of zero, no disparity change occurs for the next coded word.
- If a code word has a disparity option +/− 2, a disparity is selected that prompts a sign change for the next word. To achieve this, there must be two coding options for words, which do not have an equal number of zeros and ones.

Table 6: Rules for running disparity coding

Previous RD	Disparity of Code word	Disparity chosen	Next RD
−1	0	0	−1
−1	+/− 2	+2	+1
+1	0	0	+1
+1	+/− 2	−2	−1

Table 7: 5b/6b code table

Input	EDCBA	RD = −1	abcdei	RD = +1
D.00	00000	100111		011000
D.01	00001	011101		100010
D.02	00010	101101		010010
D.03	00011		110001	
D.04	00100	110101		001010
D.05	00101		101001	
D.06	00110		011001	
D.07	00111	111000		000111
D.08	01000	111001		000110
D.09	01001		100101	
D.10	01010		010101	
D.11	01011		110100	
D.12	01100		001101	
D.13	01101		101100	
D.14	01110		011100	
D.15	01111	010111		101000
D.16	10000	011011		100100
D.17	10001		100011	
D.18	10010		010011	
D.19	10011		110010	
D.20	10100		001011	
D.21	10101		101010	
D.22	10110		011010	
D.23	10111	111010		000101
D.24	11000	110011		001100

Input	EDCBA	RD = −1	abcdei	RD = +1
D.25	11001		100110	
D.26	11010		010110	
D.27	11011	101110		001001
D.28	11100		001110	
D.29	11101	101110		001110
D.30	11110	011110		100001
D.31	11111	101011		010100

Table 7 above shows how the original 5-bit code words are coded into 6-bit code words. Each new 6-bit code word contains either:

- 3 zeros and ones
- 2 ones and 4 zeros or
- 4 zeros and 2 ones.

The 6-bit code word in column RD = +1 can be created easily by inverting all bits of the code word in column RD = −1.

Table 8: 3b/4b code table

Input	HGF	RD = −1	fghj	RD = +1
D.x.0	000	1011		0100
D.x.1	001		1001	
Dx.2	010		0101	
D.x.3	011	1100		0011
D.x.4	100	1101		0010
D.x.5	101		1010	
D.x.6	110		0110	
D.x.P7	111	1110		0001
D.x.A7	111	0111		1000

Table 8 shows the coding scheme from 3-bit to 4-bit.

Note that Tables 7 and 8 each contain one exception to the rule. The word codes 111000 (RD = −1) and 000111 (RD = +1) in Table 7 (EDCBA column value 00111) each contain the same number of zeros and ones. The same applies for the word codes 0011 and 1100 in Table 8 (HGF column value 011).

High-speed interfaces like PCI Express, Serial ATA, Display Port, Fibre Channel Gigabit, Ethernet and DVB make use of 8b/10b-encoding, which also supports AC-coupling. This makes clock recovery much easier. Clock recovery with a PLL clock generator is required in all scenarios in which no separate clock signal is sent with the data. The PLL of the data receiver needs to synchronize to the data signal transitions to allow safe sampling of incoming data.

High-speed USB, and the slower modes, make use of one differential pair with signal lines D+ and D− for data transmission, which allows half duplex data transmission. USB 3.x makes use of two differential pairs. This allows data flow in both directions in full duplex mode.

Figure 7 shows the termination of the D+ and D− lines. On both sides of the connection a 45 Ω single-ended termination to ground is implemented. This results in a 90 Ω differential termination of the signal lines. In practice, the 45 Ω serial resistor behind the LS/HS drivers are switched to ground. By doing so, the serial resistor functions as 45 Ω termination for this high-speed use case.

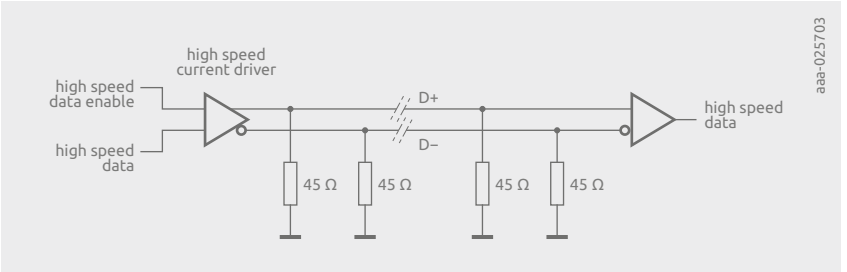

Figure 7 | Basic termination scheme for USB HS-Mode

The high-speed drivers are implemented as switched current sources that deliver 17.78 mA in single-ended high state. Figure 8 shows this basic driver structure. The high-state voltage at the 45 Ω resistors in parallel operation, V_{SEhigh}, is given by:

$$V_{SEhigh} = \frac{17.78\ mA}{22.5\ \Omega} = 400\ mV$$

The nominal differential voltage swing on the D+/D− signal pair is therefore ± 400 mV.

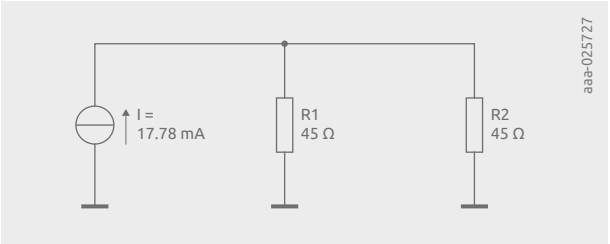

Figure 8 | HS 17.78 mA current source attached to each signal line (D+/D–)

In Figure 9 the coupling of the two differential signal pairs for the SuperSpeed signals RX and TX is depicted. At every transmitter side, the TX lines contain capacitors that realize AC-coupling for both differential connection lanes. The nominal capacitance of these capacitors is 100 nF. The Figure shows the cable connection of a host and a USB device that is plugged into mated connectors.

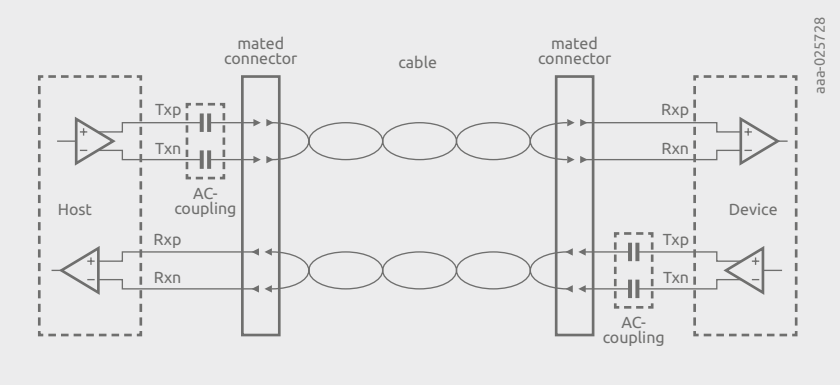

Figure 9 | SuperSpeed Rx and Tx connection scheme up to USB 3.1

USB 3.2 adds the option to place additional 330 nF capacitors at the data inputs RXp and RXn and a 250 kΩ termination to ground at the cable side of the capacitors as an extension of the USB 3 standard. The fully AC-coupled SuperSpeed interface setup is illustrated in Figure 10. This setup becomes mandatory with USB 4, as described in chapter 7.1.5.

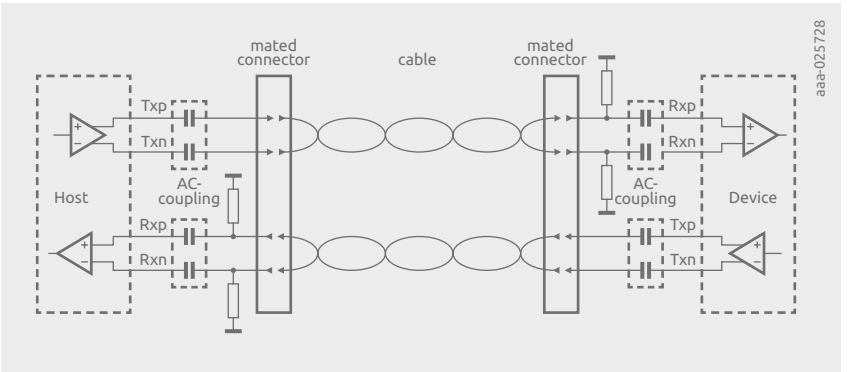

Figure 10 | Fully AC-coupled USB SuperSpeed interface with second AC coupling capacitance for the Rx interface

7.1.4 USB 3 Gen 1 and Gen 2 eye diagrams

If a connection is set up via a USB 3 Gen 1 or USB Gen 2 connection, link training is performed as a sequence with the following steps:

1. Configuring and initializing of link.
2. Bit-lock and symbol lock.
3. Rx equalization training.
4. Lane polarity inversion.
5. Block alignment (USB 3 Gen 2 only).

Training sequences are always 8b/10b encoded and not scrambled. Table 9 shows the most important normative requirements for USB 3 Gen 1 and Gen 2 transmitters.

Table 9: Basic requirements for a USB 3 transmitter

Symbol	Explanation	Gen 1, 5 Gbit/s	Gen 2, 10 Gbit/s
UI	Unit Interval	199.94 ps (min) 200 ps (nom) 200.06 ps (max)	99.97 ps (min) 100 ps (nom) 100.03 ps (max)
$V_{TX\text{-}Diff\text{-}PP}$	Differential peak to peak TX voltage swing	0.8 V (min) 1 V (nom) 1.2 V (max)	0.8 V (min) 1 V (nom) 1.2 V (max)
$V_{TX\text{-}DE\_RATIO}$	TX de-emphasis	3 dB (min) 4 dB (max)	3-tap FIR equalizer

Symbol	Explanation	Gen 1, 5 Gbit/s	Gen 2, 10 Gbit/s
$R_{TX-DIFF-DC}$	DC differential impedance	72 Ω (min) 90 Ω (nom) 120 Ω (max)	72 Ω (min) 90 Ω (nom) 120 Ω (max)
$C_{AC-COUPLING}$	AC coupling capacitor	75nF–200nF	75nF–265nF
T_{TX-EYE}	Transmitter eye width	0.625 UI (incl. all jitter sources)	0.625 UI (incl. all jitter sources)

Table 10 is the equivalent list for the receiver side of the super-speed USB interface. The minimum height of the receiver eye is quite low. The open width is also much smaller compared to USB super-speed.

Table 10: Basic requirements for USB 3 receiver

Symbol	Explanation	Gen 1, 5 Gbit/s	Gen 2, 10 Gbit/s
UI	Unit Interval	199.94 ps (min) 200 ps (nom) 200.06 (max)	99.97 ps (min) 100 ps (nom) 100.03 ps (max)
$V_{RX-DIFF-PP-POST-EQ}$	Differential peak to peak RX voltage swing	100 mV (min)	70 mV (min)
RX equalizer	receiver equalizer	0 dB–6 dB	0 dB–6 dB
T_j	total jitter	0.66 unit intervals	0.714 unit intervals
$R_{RX-DIFF-DC}$	DC differential impedance	72 Ω (min) 90 Ω (nom) 120 Ω (max)	72 Ω (min) 90 Ω (nom) 120 Ω (max)
$C_{AC-COUPLING}$	AC coupling capacitor	75 nF–200 nF	75 nF–265 nF

Figure 11 shows the receiver mask for 5 Gbit/s, and Figure 12 depicts the mask for 10 Gbit/s. The mask in the USB 3 Gen 1 scenario has a minimum eye height of 100 mV whereas the eye height in USB 3 Gen 2 scenario is only 70 mV. The minimum eye width is 0.34 unit intervals, compared with 0.286 unit intervals in the 10 Gbit/s scenario. The shape of the mask is also different. In the 5 Gbit/s scenario the mask has the shape of a rhombus whereas the shape in the 10 Gbit/s scenario is similar to the USB 2.0 scenario, with a 0.1-unit interval width for the upper and lower mask borders.

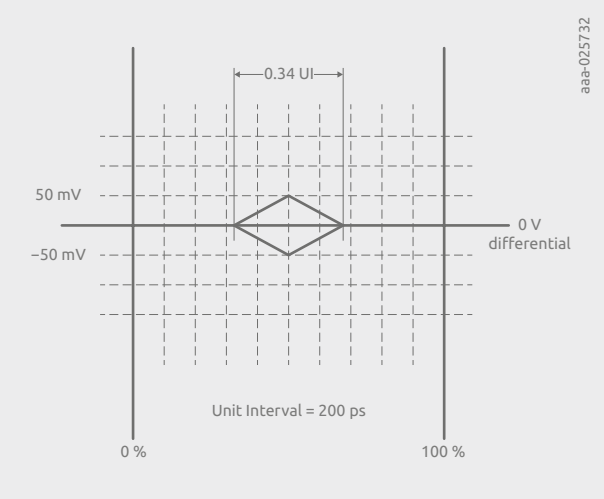

Figure 11 | Mask diagram of USB 3 Gen 1 scenario; 5 Gbit/s

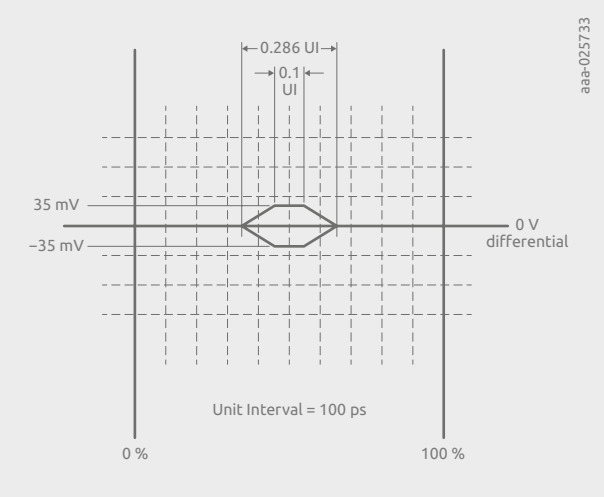

Figure 12 | Mask diagram of USB 3 Gen 2 scenario; 10 Gbit/s

7.1.5 USB 4 and Thunderbolt interfaces

The latest super-speed data standard at the time publication is USB 4 Version 2 (Gen 4). It uses the USB Type-C environment to achieve data transfer at up to 80 Gbps.

Its key characteristics are:
- symmetric (80/80 Gbps) or optional asymmetric (120/40 Gbps) operation through lane reconfiguration
- alignment with DisplayPort 2.1 and PCI Express Rev. 4.

The standard is described in detail below.

USB 4 V1 (Gen 3)

The first version of the USB 4 standard was introduced in 2019.[1] The main changes from USB 3.2 were:

- doubling the data rate from 20 to up to 40 Gbps
- backwards compatibility with USB 3.2, USB 2.0 and Thunderbolt 3
- tunneling of other standards like USB 3.x, PCIe and DP as packets through the USB 4 transport.

USB 4 Gen 2 (10 Gbps/port) supports cables up to 2 m, with a budget of 12 dB, while USB 3.2 Gen 2 (10 Gbps/port) supports only 1 m cables, with a 6 dB budget. This came with a recommended reduction of the total insertion loss of the router assembly to 5.5 dB @ 10 GHz for Gen 2. For Gen 3, the total recommended insertion loss of the router assembly is 7 dB @ 10 GHz.

Table 11: USB 4 electrical compliance test points

Test Point	Description	Comments
TP1	Transmitter IC output	Not used for electrical testing.
TP2	Transmitter port connector output	Measured at the plug side of the connector.
TP3	Receiver port connector output	Measured at the receptacle side of the connector. All the measurements at this point shall be done while applying reference equalization function.
TP3'	Receiver port connector input	Measured at the plug side of the connector.
TP4	Receiver IC input	Not used for electrical testing.

1 www.usb.org/sites/default/files/2019-09/USB-IF_USB4%20spec%20announcement_FINAL.pdf

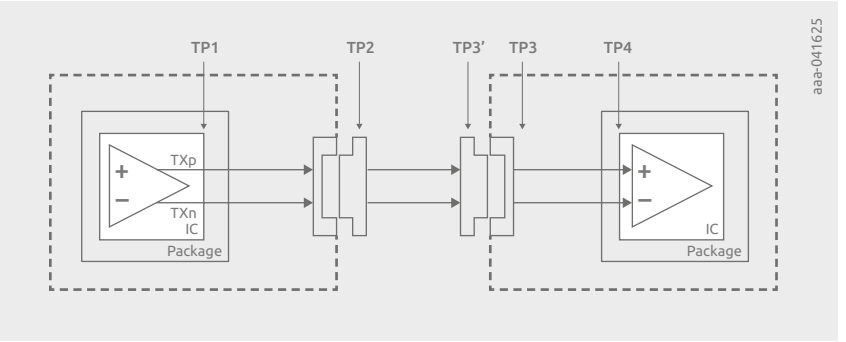

Figure 13 | USB 4 compliance points definition

The AC-coupling capacitances between connector and Rx ports introduced in USB 3.2 became mandatory with USB 4 at 300-363 nF. Tx interfaces have AC-coupling capacitances between 135 nF and 265 nF.

Since the line between TP2 and TP3 is now fully AC-coupled, 200-242 kΩ pull-down resistors have been added at the Rx side for discharge. Pull-down resistors at the Tx side are optional.

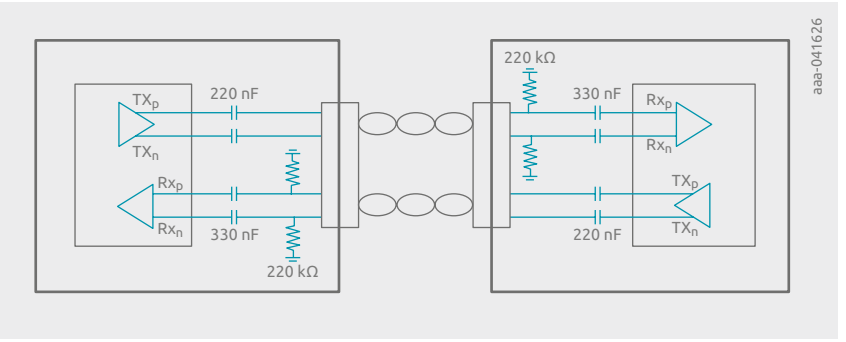

Figure 14 | Topology of fully AC-coupled USB SuperSpeed lines (USB4, USB 3.2)

For USB 4 operation, insertion-loss and return-loss budgets are evaluated at 10 GHz, the fundamental of the highest Gen 3 data rate.

Transmitter and receiver differential return-loss measurements are referenced to a single-ended impedance of 42.5 Ω, resulting in a differential impedance of 85 Ω.

Time-domain measurements such as eye diagrams are made with a single-ended impedance of 50 Ω.

From the perspective of ESD protection, it should be mentioned that the AC-coupling capacitances do not protect against fast transients such as ESD pulses.

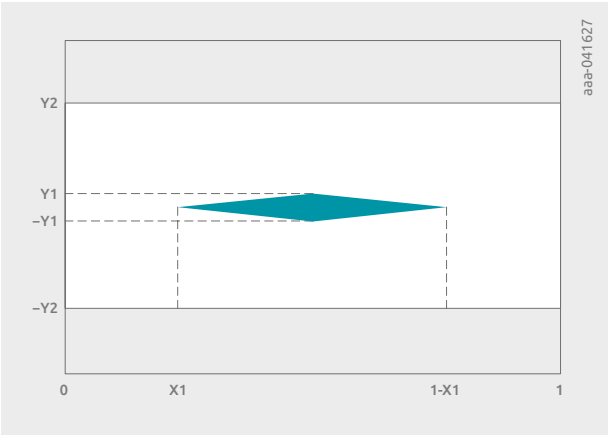

Figure 15 | USB Gen3 TX mask notations

Table 12: USB Gen3 transmitter specifications at TP3

Symbol	Description	Min	Nom	Max	Units	Comments
UI	Unit Interval	–	50	–	ps	
TJ	Total Jitter	–	–	0.60	UI pp	Note 1
X1	TX eye horizontal deviation	–	–	0.23	UI	Note 1
Y1	TX eye inner height (one-sided voltage opening of the differential signal)	53	–	–	mV	Note 1
Y2	TX eye outer height (one-sided voltage opening of the differential signal)	–	–	650	mV	Note 1

Note 1:
See USB4 specification for measurement details (https://usb.org/document-library/usb4r-specification-v20)

USB 4 Version 2.0 (Gen 4)

USB 4 Version 2.0 (Gen 4), introduced in 2022 [5], doubled the maximum data rate again. Three-level pulse amplitude modulation (PAM3) was introduced to increase the data rate to 25.6 Gbaud per lane, giving a Nyquist frequency of 12.8 GHz. It is recommended that a router assembly has a total insertion loss budget of less than or equal to 9.5 dB at 12.8 GHz.

The topology of a Type-C interface for USB 4 Gen 4 remains unchanged from Gen 3 (see Figure 14).

Impact of higher data rates on system-level ESD robustness

Increasing data rates make protecting high-speed data lines more important, for several reasons.

- High IC-level on-chip ESD robustness typically increases RF losses, for example due to higher circuit capacitances. In many situations this budget for RF losses is no longer available at higher data rates.
- At the same time, the RF insertion loss budget for external ESD protection is reduced. Decreasing ESD device areas to reduce capacitance will increase clamping, for example.
- SuperSpeed data lines make frequent use of re-timer or re-driver devices. These are typically positioned closer to the ESD protection device to improve signal integrity. The reduced trace length increases the clamping voltage at the protected IC.

All three factors increase the trend for the weakest link in the ESD protection chain to typically be the IC failing due to the clamping voltage while the on-board ESD protection device remains undamaged.

Most ICs fail due to the energy content of the clamping voltage, but some also fail as a result of gate-oxide overstress due to a high-voltage 1st ESD peak.

The third factor, the reduced trace length between on-board ESD protection and protected IC, can lead to fails in ESD tests which previously passed, although IC and ESD protection are unchanged.

We discuss the impact of the trace length between on-board ESD protection and IC in-depth when looking at System Efficient ESD Protection (SEED) in Chapter 9.

7.1.6 USB Type-C

The user-friendly 24-pin USB Type-C connector allows plugs to be reversible. The innovative connector type supports up to USB 4 2.0 (Gen 4) speeds of 80 Gbit/s, as well as USB PD R3.2 power delivery. Full-feature cables are electronically marked with an identification IC. Alternate modes can be set up via the dedicated configuration channels, using vendor defined messages (VDMs).

The Type-C connector can support various other standards besides USB. These include Display Port, Thunderbolt, MHL, PCI Express and Base-T Ethernet. Various dongles that convert from USB Type-C to legacy connectors or other interface standards such as HDMI are available on the market.

In Table 13 the pin assignment of a USB Type-C connector is listed. Figure 16 shows the front view of a Type-C receptacle. The 24 pins are organized in two groups of 12 – group A and group B. Pins are available for four differential pairs with SuperSpeed operation (two lanes each for RXP/RXN and TXp/TXn). There are also two pins for a USB 2.0 lane pair (Dp/Dn), two configuration channel pins (CC1 and CC2) and two sideband usage (SBU) pins. Additionally, four Ground and four V_{BUS} pins ensure low resistance for the power path.

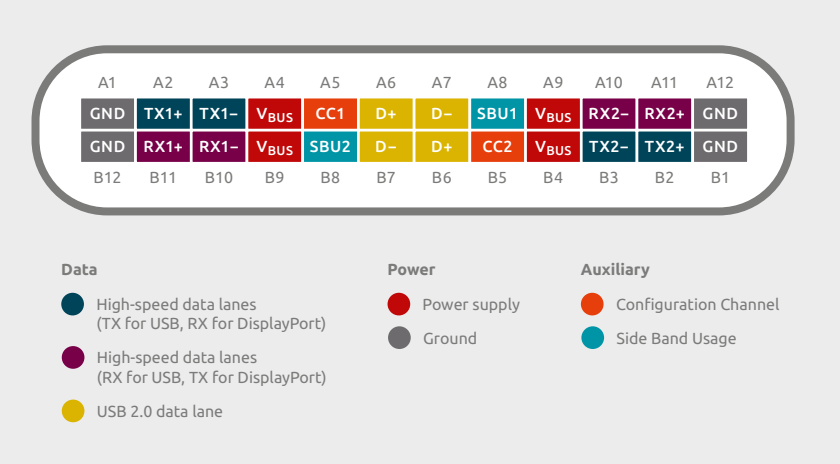

Figure 16 | Pinout of a USB Type-C connector

Table 13: USB Type-C pin assignment

Pin number	Signal name	Explanation
A1	GND	Ground
A2	SSTXp1	Super Speed differential TX pair 1, positive signal
A3	SSTXn1	Super Speed differential TX pair 1, negative signal
A4	V_{BUS}	Bus Power line
A5	CC1	Configuration Channel 1
A6	Dp1	USB 2.0 differential pair 1, positive signal
A7	Dn1	USB 2.0 differential pair 1, negative signal
A8	SBU1	Sideband Usage signal 1
A9	V_{BUS}	Bus Power line
A10	SSRXn2	Super Speed differential RX pair 2, negative signal
A11	SSRXp2	Super Speed differential RX pair 2, positive signal
A12	GND	Ground
B1	GND	Ground
B2	SSTXp2	Super Speed differential TX pair 2, positive signal
B3	SSTXn2	Super Speed differential TX pair 2, negative signal
B4	V_{BUS}	Bus Power line
B5	CC2	Configuration Channel 2
B6	Dp2	USB 2 differential pair 2, positive signal
B7	Dn2	USB 2 differential pair 2, negative signal
B8	SBU2	Sideband Usage signal 2
B9	V_{BUS}	Bus Power line
B10	SSRXn1	Super Speed differential RX pair 1, negative signal
B11	SSRXp1	Super Speed differential RX pair 1, positive signal
B12	GND	Ground

As soon as a connection is established, the orientation of the cable connection is detected via the CC pins. The Type-C cable has only one physical CC wire. With this single connection both ends of the cable can detect the appropriate SuperSpeed lines needed for data exchange.

For example, connecting between a downstream facing port (DFP) and an upstream facing port (UFP) follows this process:

1. DFP to UFP attach / detach detection.
2. Plus orientation / cable twist detection.
3. Initial DFP-to-UFP (host to device) and power relationship detection.
4. USB Type-C V_{BUS} current detection and usage.
5. USB power delivery (PD) communication.
6. Discovery and configuration of functional extensions.

Figure 17 shows a DFP to UFP connection. On the DFP side, pull-up resistors Rp are implemented to achieve a positive supply voltage. On the other end of the cable, pull-down resistors are connected to ground.

Note that, by default, a current source can be configured instead of using Rp pull-up resistors. The node with the higher voltage of the two CC pins indicates the direction of the connection. Ra is available for powered cables and audio adapters, as shown in Table 16 below. The Rp value can detect 5 V-current capability.

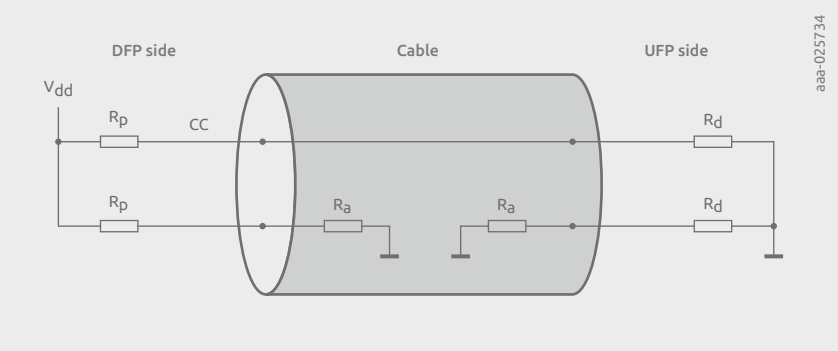

Figure 17 | DFP-UFP model connection

Table 14 shows values for the pull-up resistor Rp and the related power rating for either a 5 V or 3.3 V supply connected to the pull-up as supply voltage.

Table 15 defines how the pull-down resistor Rd is specified. The nominal termination is a 5 kΩ resistor. Voltage clamping does not allow detection of power capability. For this function the tolerance of Rd needs to be at least ±10%.

Table 14: Down-stream port (DFP) Rp requirements

DFP Dedication	Current Source to 1.7 V – 5.5 V	Pull-up resistor to 4.75 V – 5.5 V	Pull-up resistor to 3.135 V – 3.465 V
Default USB power	80 µA +/– 20%	56 k +/– 20%	36 +/– 20%
1.5 A/5 V	180 µA +/– 8%	22 k +/– 5%	12 +/– 5%
3.0 A/5 V	330 µA +/– 8%	10 k +/– 5%	4.7k +/– 5%

Table 15: Up-stream port (UFP) Rd requirements

Rd implementation	Nominal value	Power detection capability	maximum voltage at the CC pin
+/– 20% voltage clamp	1.1 V	no	1.32 V
+/– 20% resistor to GND	5.1 kΩ	no	2.18 V
+/– 10% resistor to GND	5.1 kΩ	yes	2.04 V

The Ra termination resistor has a nominal resistance of 1 kΩ, as shown in Figure 17. It is often applied via a junction field-effect transistor (JFET) that limits the current following the detection process, as shown in Figure 18.

As soon as the pitch-off voltage of the depletion FET is reached, the current increases the voltage level in Ra at the source of the depletion FET until it clamps the current to a maximum value. Thus, power loss is reduced whenever the 5 V supply voltage VCONN is switched to the CC line.

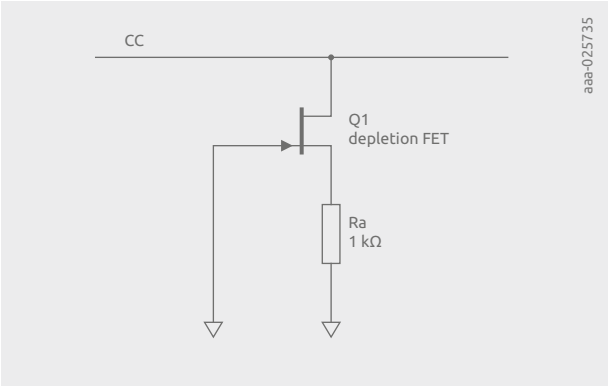

Figure 18 | Ra termination solution

Table 16 lists the states that result from CC line termination in a DFP-UFP connection.

Table 16: CC connection model for a DFP-UFP scenario

CC1	CC2	State
open	open	Nothing attached
Rd	open	UFP attached
open	Rd	UFP attached
Ra	open	Powered cable, no UFP attached
open	Ra	Powered cable, no UFP attached
Ra	Rd	Powered cable and UFP attached
Rd	Ra	Powered cable and UFP attached
Rd	Rd	Debug accessory Mode attached
Ra	Ra	Audio adapter accessory Mode attached

Short-circuit from V_{BUS} to data lines

ESD protection scenarios for SuperSpeed lines

Looking at the USB Type-C interface pinout, the lines adjacent to V_{BUS} are CC/SBU and SuperSpeed. USB PD allows power supply of up to 5 A and 20 V; and up to 48 V when using the Extended Power Range (EPR). A frequent discussion point concerns the impact of a short-circuit condition of the V_{BUS} line to a neighboring SuperSpeed line.

Although the USB Power Delivery specification has a number of safety measures to safeguard against fault conditions, concerns remain, that customers may be using power supplies or connectors which are not USB-PD compliant. Nevertheless, it can be useful to have a look at the PD specification – and to buy only USB-PD compliant power supplies.

Looking at the USB-PD specification [1], a source will provide 5 V in the 'default contract' on being plugged in. Setting a higher voltage rating will need negotiation between source and sink, thus a voltage greater than 5 V requires an existing connection.

When a USB Type-C connector is unplugged, a USB Detach is detected using CC detection (see Chapter 7.1.7.4 in [1]). In this case, the source transitions to vSafe0V at a maximum of 0.8 V in 650 ms (max tSafe0V), while vSafe5V is reached after no longer than 275 ms (see Table 7.25 in [1]).

Chapter 7.1.7.1 describes how sources in the Standard Power Range up to 20 V shall implement overcurrent protection. The USB-PD specification offers two options, either Hard Reset, where first vSafe5V and then vSafe0V are reached within the time frames given above, or Error Recovery, which is defined in the USB Type-C specification (4.5.2.2.2 in [2]), where the source will transition into the Unattached.SRC state, where the requirements 4.5.2.2.7.1 are that the port shall not drive V_{BUS} (or VCONN).

The USB-PD and Type-C specifications provide several safety measures. Consequently, a series of fault conditions need to come together for a situation to arise in which V_{BUS} shorts to neighboring pins.

What is the best approach to designing a SuperSpeed interface that is robust to short-circuit? Looking at the SuperSpeed interface shown in Figure 19, we have two possible placement positions for the ESD protection: between connector and AC-coupling capacitance (position A), and between the AC-coupling capacitance and the protected IC (position B):

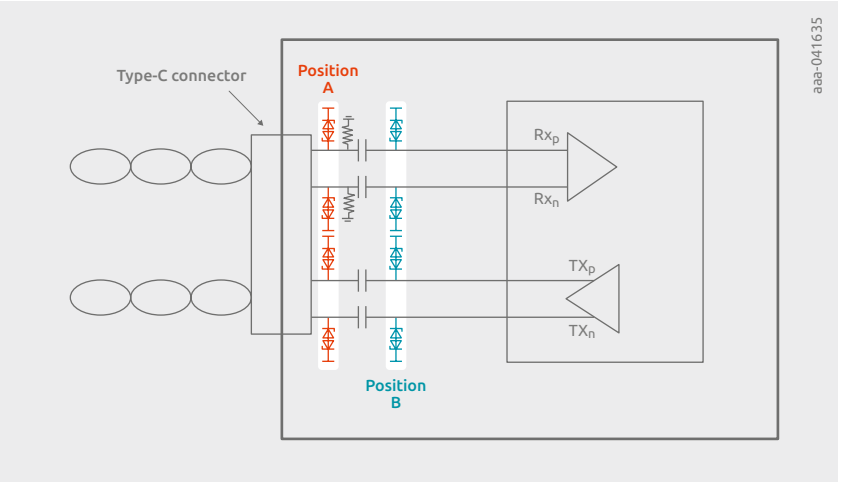

Figure 19 | Two possible positions for ESD protection in a SuperSpeed interface

As we will see, the conventional rule that ESD protection should be placed as close as possible to the connector is no longer valid. To be more precise, it would still be valid if the same ESD protection device is compared in both positions.

Two reasons can seem position A appear to look better – the available inductance between ESD protection and the protected IC is maximized, and the AC-coupling capacitance is protected against ESD. As we will see below, the increase in inductance is outweighed by the disadvantages of having a higher-voltage protection device.

Assuming a V_{BUS} voltage of 20 V, we would place a 20 V ESD protection device in position A. If we want to be prepared for the worst-case maximum level of 21.55 V [1], we will place a 22 V protection device in position A to ensure that the protection device does not turn on in the event of a short-circuit condition. As we will see, this will significantly reduce the protection to the protected IC, against both ESD strike conditions and short-circuit conditions, compared to a low-voltage device in position B.

Robustness of AC coupling capacitances against ESD strikes

Nexperia has investigated [4] several 0402" AC-coupling capacitances used in reference designs and found them all to be ESD robust to more than 40 A TLP – which corresponds a 20 kV IEC 61000-4-2 pulse (for failures on the 2nd peak). In these tests, the 330 nF capacitor showed no signs of damage up to 60 A TLP (corresponding to 30 kV IEC61000-4-2) while for the 220 nF capacitor, no damage was seen up to 40 A TLP (corresponding to 20 kV IEC61000-4-2). The 220 nF capacitor was ultimately damaged at 55 A TLP.

Based on customer feedback, Nexperia has also evaluated 25 V rated 220 nF 0201" AC coupling capacitances from two manufacturers. The measurement of the less robust capacitance is shown in Figure 20 and 21. First, a failure level was established (blue measurement), a new device was stressed then five times with TLP pulses up to 22 A 1/100 ns TLP, which was below this degradation level. This device did not show any degradation during these runs. For the capacitance from the second manufacturer, five runs up to 25 A 1/00 ns did not show any degradation.

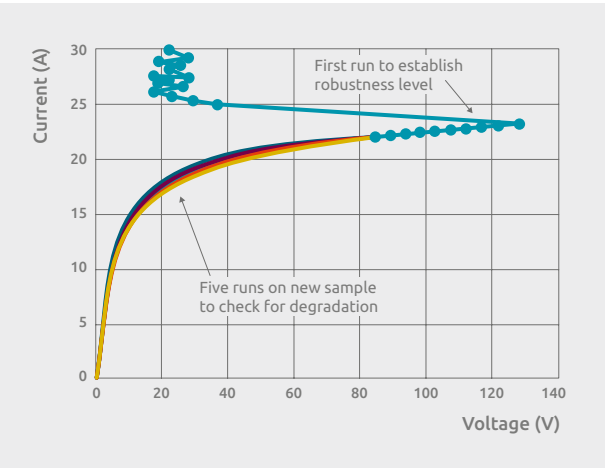

Figure 20 | Testing a 25 V rated 220 nF 0201" sample to degradation (blue measurement) and stressing a new sample five time with TLP slightly below the degradation level (up to 22 A 1/100 ns TLP). This was the least robust device in our investigations.

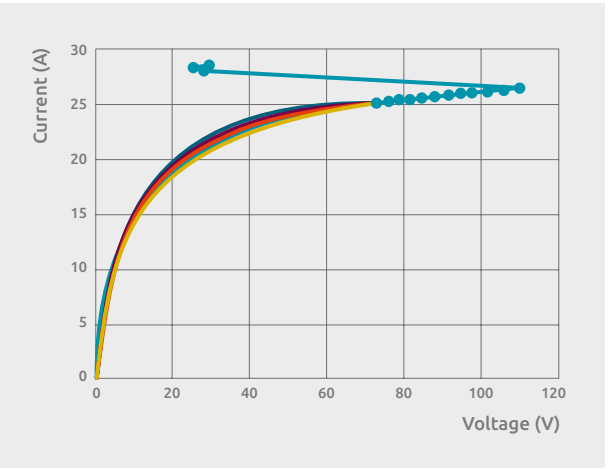

Figure 21 | Testing a 25 V rated 220 nF 0201" sample from a different manufacturer to degradation (blue measurement) and stressing a new sample five time with TLP slightly below the degradation level (up to 25 A 1/100 ns TLP).

In the next run, Nexperia have tested samples of capacitances from both manufacturers with 0.6/5 ns very-fast TLP up to 120 A but could not find any signs of degradation.

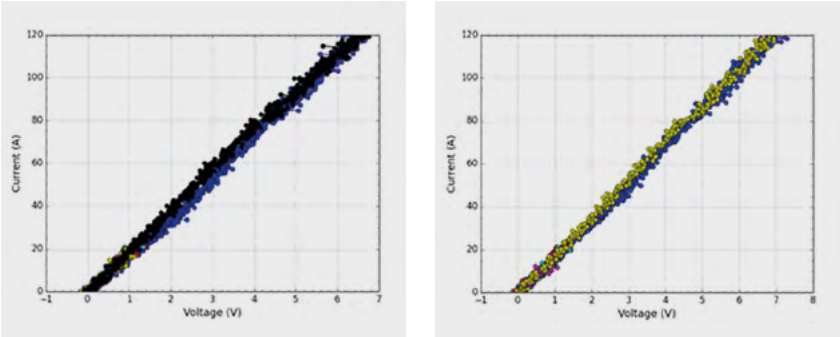

Figure 22 | Testing two 25 V rated 220 nF 0201" capacitances with 0.6/5 ns very-fast TLP. No sign of degradation was seen up to 120 A very-fast TLP.

Since the investigated AC coupling capacitances were robust up to 120 A with a 600 ps rise time, we can conclude that degradation due to an ESD pulse happens because of the energy content rather than the peak voltage. This allows to see the 22 A 1/100 ns TLP trials as equivalent to an 11 kV IEC 61000-4-2 pulse.

In other words, the robustness of all investigated AC coupling capacitances exceeded level 4 of an IEC 61000-4-2 contact discharge.

Comparing the TLP robustness of the investigated capacitors to that of typical SuperSpeed USB ICs (as presented in the next section) indicates that the capacitors are unlikely to be the weakest link in the event of an ESD strike. As we will see below, the weakest link is likely to be the clamping voltage seen by the protected IC.

Impact on the ESD stress to the protected IC

We have investigated a number of transceiver ICs (re-timer and re-driver devices) for SuperSpeed data lines and found that their TLP characteristic closely resembles a forward-biased diode in series with a resistor. This means that the on-chip ESD protection of these ICs becomes conductive at very low voltages between 1 V and 1.5 V. Any external ESD protection device needs to have a low trigger voltage to limit the ESD current flowing into the protected IC before the IC is damaged.

An example is shown in Figure 23A+B.

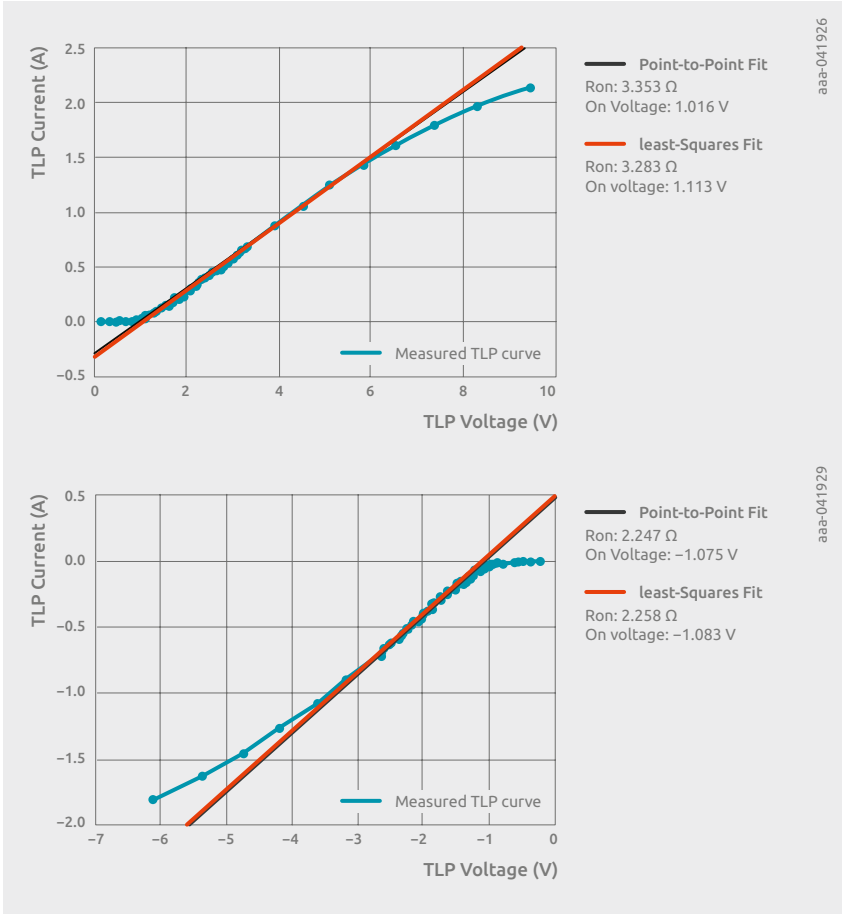

Figure 23A | 1/100 TLP behavior of a typical USB SuperSpeed IC. The on-chip protection becomes conductive already at ~ 1 V.

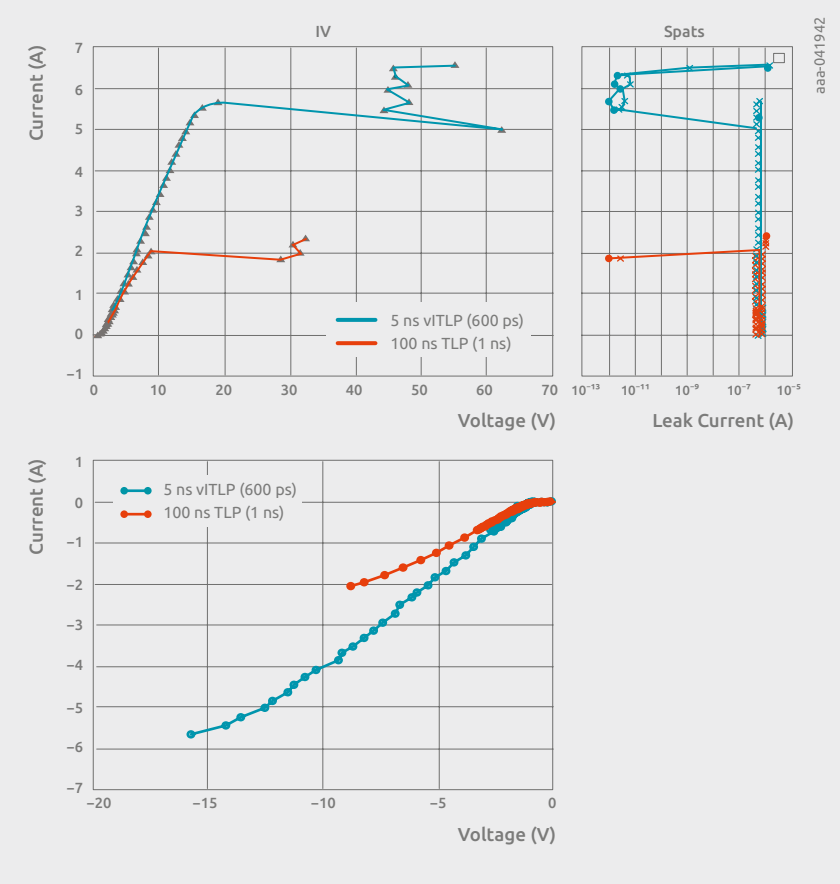

Figure 23B | 1/100 TLP and 0.6/5 ns vfTLP leakage current measurements to check for damage of the on-chip ESD protection.

Summing up Figure 23:

- Like all investigated SuperSpeed ICs, the internal ESD protection turns on at around 1 V
- The on-chip ESD protection of the IC is damaged at 2 A 1/100 ns TLP
- The on-chip ESD protection of the IC is damaged at ~ 5 A 0.6/5 ns vfTLP. This higher level for vfTLP indicates that the IC is more sensitive to the energy content of the pulse rather than the peak clamping voltage

The system described above is sensitive to remaining clamping after ESD protection. We have measured more robust systems which could handle up to 6 A TLP but these systems become conductive at around 1 V and start to shunt transients as well.

To compare how such a system reacts to high-voltage ESD protection devices in position A compared to low-voltage ESD protection devices in position B, we have compared measurements obtained using a test set-up with those from SEED simulations [3].

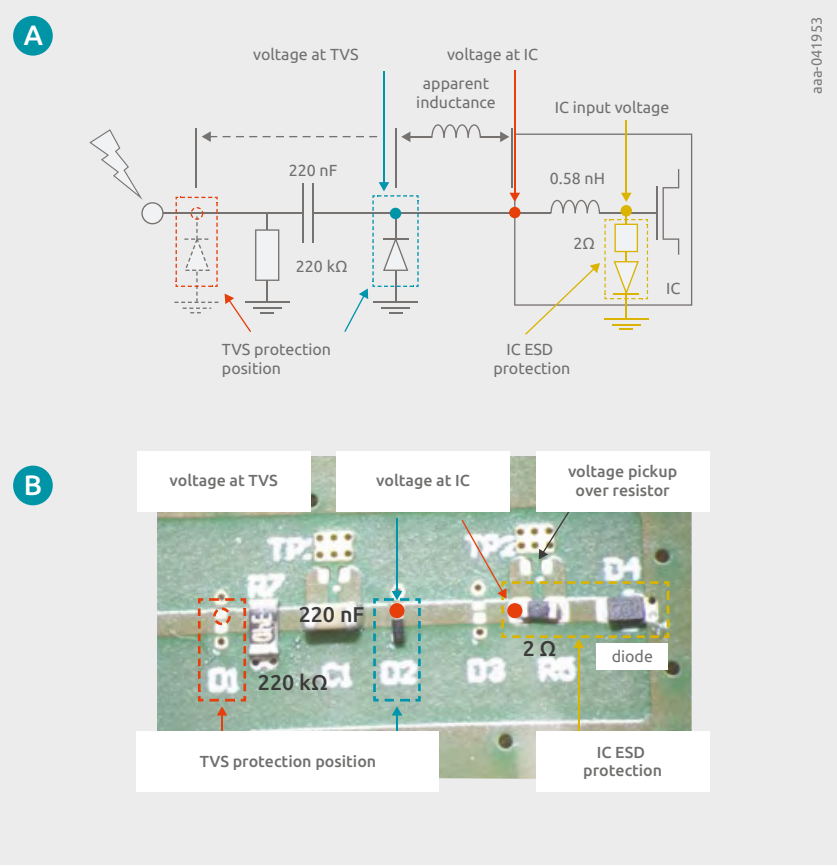

Figure 24 | Test interface for an AC-coupled SuperSpeed data line with, from left to right: connector (not shown), ESD footprint for position A, pull-down resistor, AC-coupling capacitance, ESD footprint for position B, IC replacement circuit (resistor plus diode).

Four different ESD protection devices with a 1 V rating (1–4) were placed in position B, two 18–24 V rated ESD protection devices (5–6) were placed in position A.

TLP and peak clamping voltages are shown in Figure 25.

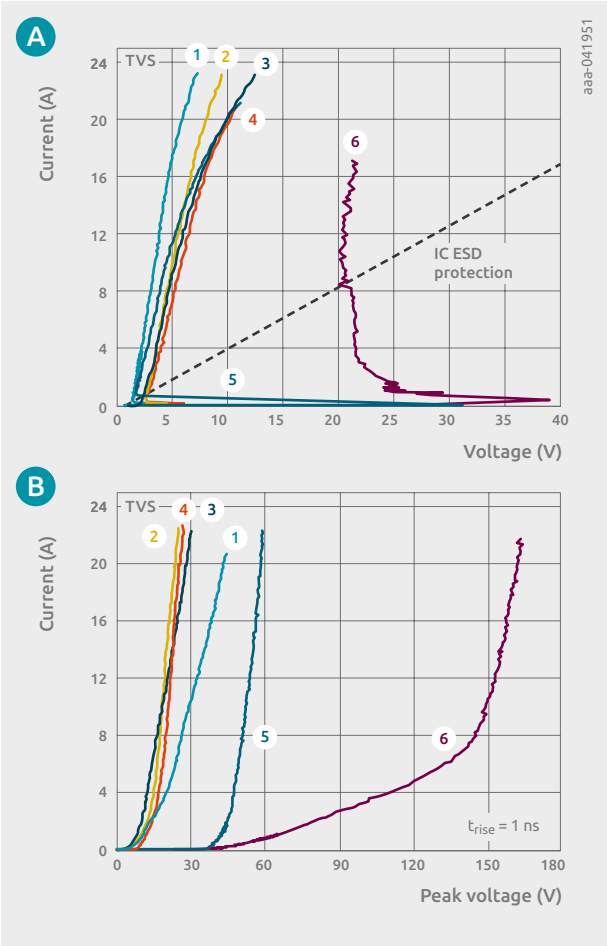

Figure 25 | Comparison of TLP curves A and peak clamping voltages B for ESD devices with 1 V rating (1–4) in position B and devices with 18–24 V rating in position B.

The difference between the TLP currents flowing through the IC replacement circuit for positions A and B are notable, as shown in Figure 26.

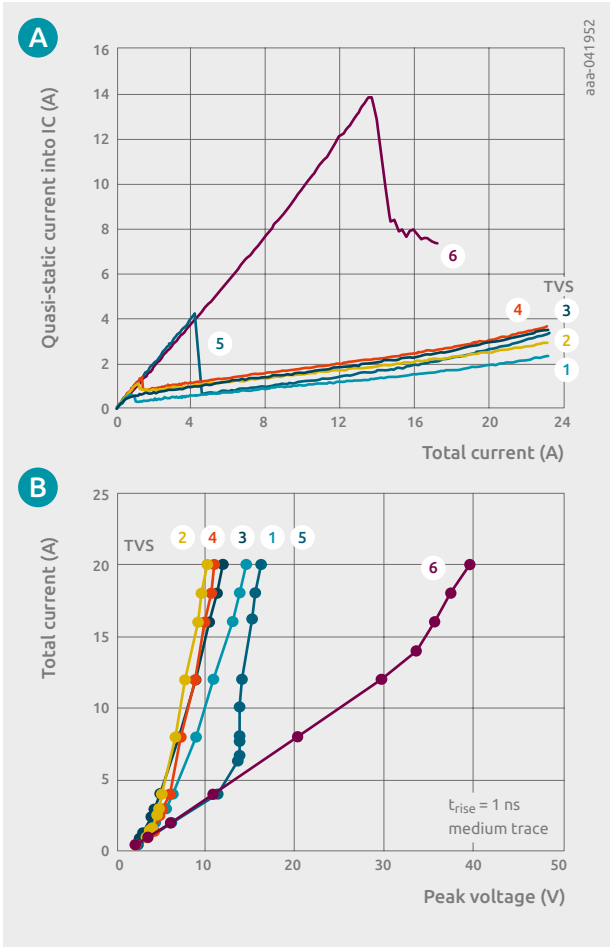

Figure 26 | TLP current A and peak voltage B seen by the IC

Device 5 might protect some ICs which can survive more than 4 A TLP flowing into the IC before the device triggers. The IC in Figure 23 would not survive this pulse. In any case, the overall transient current stress to the IC for all four protection devices in position B is significantly lower compared to position A.

Summing up, a low-voltage protection device in position B will offer better system-level ESD protection, since the ESD protection starts to protect the IC while a significantly lower transient current is flowing through the IC.

Does an AC-coupling capacitance protect against short circuits?

In short, AC-coupling capacitances are no reliable protection against short circuits of V_{BUS} to the SuperSpeed data lines. We have investigated this scenario in detail and found that in the event, that a short-circuit is applied (or removed) a transient can pass through the AC-coupling capacitance and expose the IC to surge pulses in the µs range.

For the evaluation [4], a test board was used with the IC representation circuit as described in the ESD tests above.

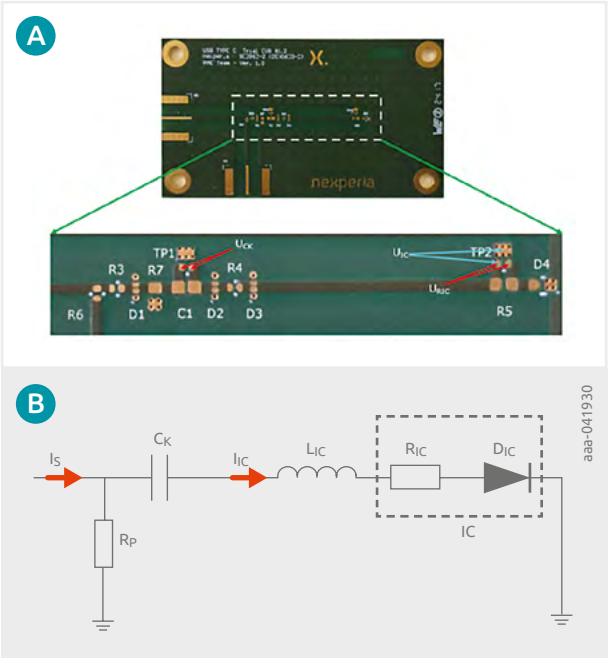

Figure 27 | A Test PCB using the elements of a SuperSpeed line and test points. B Measurement setup with high-voltage ESD in position A or no ESD protection

The short-circuit was applied using a signal-generator driving a MOSFET, which gave a rise time of ~ 50 ns.

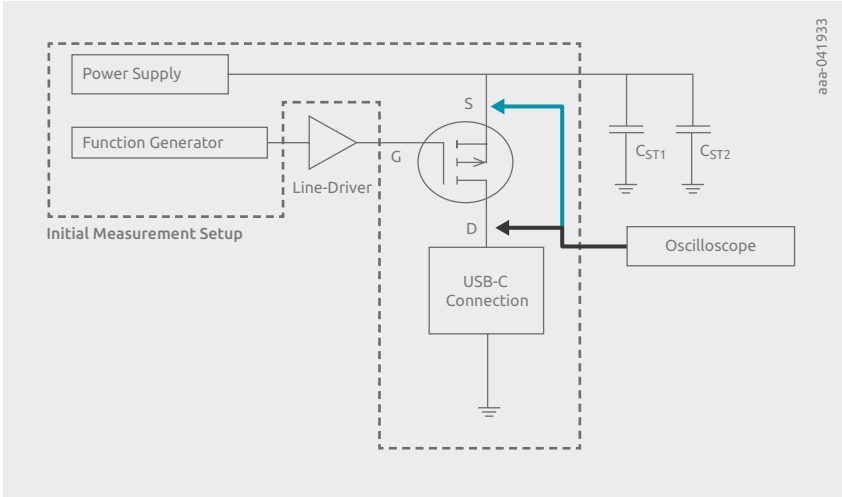

Figure 28 | Short-circuit driving circuit

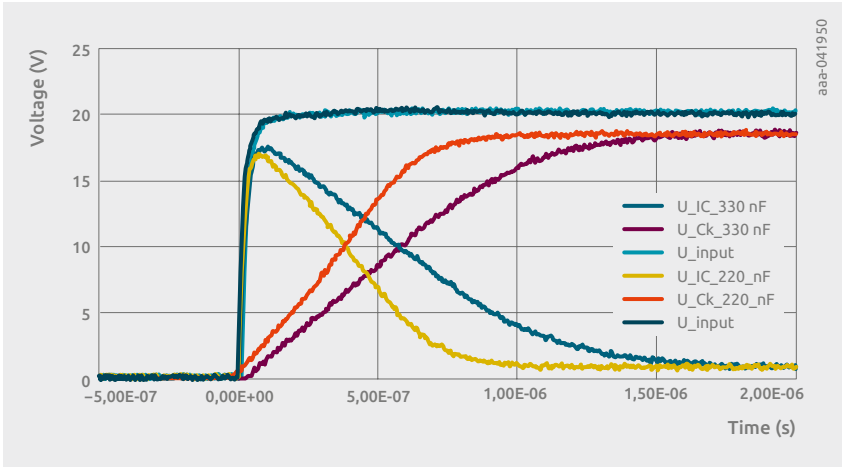

Figure 29 | Voltage waveforms for a 20 V short circuit applied to an AC coupled SuperSpeed line with 220 nF or 330 nF capacitor.

As shown in Figure 29,different waveforms result from the application of such a short circuit. The signals at the input (U_{input}) show a rise to 20 V with a rise time of a few ten nanoseconds. As to be expected, the rise time of the voltage drop over the AC coupling capacitance (U_{ck}) depends on the capacitance value. The duration of the voltage drop over the IC replacement circuit (U_{IC}) also depends on the capacitance value; both result in a surge pulse in the range of 1 µs.

Figure 30 shows the current flowing into a SuperSpeed IC over time when exposed to such a short-circuit, protected by an ESD protection device.

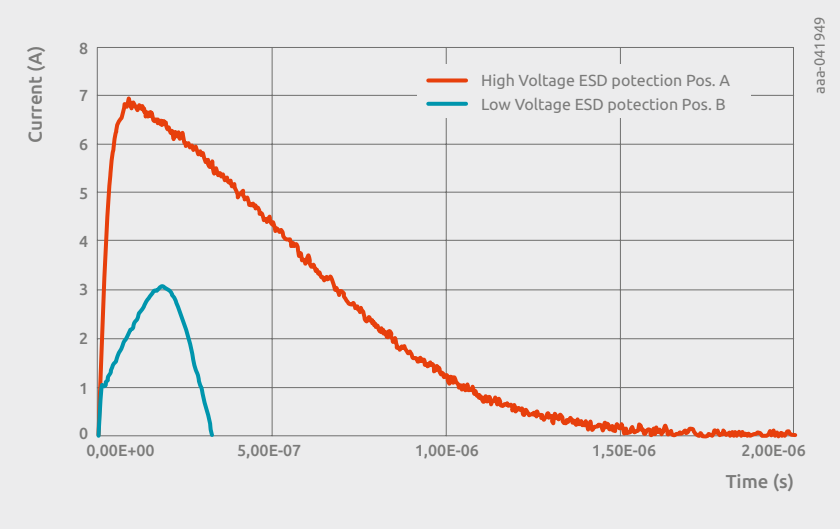

Figure 30 | Surge current through the SuperSpeed IC replacement circuit when applying a 20 V short-circuit to the AC-coupling capacitor

Using high-voltage ESD protection in position A, the application of a 20 V short-circuit to an AC-coupled SuperSpeed interface results in a surge pulse of ~ 7 A with a duration of ~ 1 µs (ten times the duration of a TLP or IEC ESD pulse). It is safe to say that no IC which can hardly handle 7 A TLP (with a pulse time an order of magnitude shorter) would survive this pulse.

Placing ESD protection > 20 V in position A might save the ESD protection from such a short-circuit condition, but it will not protect the IC against the transient when the short-circuit is applied or removed.

On the other hand, placing an 1 V ESD protection device in position B will offer a much lower and shorter pulse, thus strongly reducing the stress to the protected IC. This surge current can be further reduced by placing a resistor into the signal line. The value of this resistor needs to be balanced with the RF performance of the system.

These investigations have so far been performed for a system having V_{BUS} = 20 V. It should be noted that the new Extended Power Range (EPR) allows up to 48 V, which will further exacerbate the situation and support a more urgent recommendation for a low-voltage ESD protection in position B.

Our clear recommendation is to put a low-voltage ESD protection device in position B (as shown in Figure 19), if short-circuit conditions between V_{BUS} and SuperSpeed lines are expected:

- Typical 0402" AC coupling capacitances are ESD robust > 40 A TLP (~ 20 kV IEC61000-4-2) while typical 0201" 220 nF AC coupling capacitances are robust > 11 kV, exceeding level 4 of IEC61000-4-2.
- In case of an ESD event, the current of the remaining clamped ESD pulse is notably reduced compared to high-voltage ESD in position A.
- In case of a short-circuit event to V_{BUS}, the transient surge pulse coupling through the AC coupling capacitance when the short-circuit is applied or removed is significantly reduced compared to high-voltage ESD in position A.

ESD protection scenarios for CC and SBU lines

The other group of data lines next to V_{BUS} in a Type-C connector are the CC and SBU lines. Apart from the lower data rates, their other main difference compared to SuperSpeed lines is the lack of AC-coupling. Consequently, every overvoltage condition will be applied both to the IC with the on-chip ESD protection and to the on-board ESD protection.

If such a CC/SBU interface needs to be protected against short circuits to V_{BUS}, both the protected IC and the on-board ESD protection will be exposed to V_{BUS}, hence both need to be robust to the maximum V_{BUS} voltage. For the on-board ESD protection device, a device without or with a shallow snap-back greater than V_{BUS} can be chosen. This ensures that the on-board ESD protection is not triggered by an additional transient, followed by a latch-up by V_{BUS}, but will expose the protected IC to higher clamping voltages greater than V_{BUS} for the full duration of an ESD pulse. An on-board ESD protection device with a deeper snap-back will offer lower clamping, and thus better protection at least against the second peak of an ESD pulse. Using ESD protection with shallow snap-back, an assessment needs to be carried out to identify whether the robustness of the protected IC is high enough to achieve the desired system-level ESD robustness. SEED simulations (described in Chapter 9.2) are a valuable tool to reduce the time of such evaluations. In case the robustness of the protected IC is insufficient, it needs to be assessed which risk is higher – damage of the IC due to ESD clamping or damage of the external ESD protection due to V_{BUS}.

7.2 Video interfaces

7.2.1 HDMI interface

High-Definition Multimedia Interface (HDMI) is a digital interface for consumer and computing applications which is sometimes used in the automotive sector to connect headrest displays or dashcams. It is similar to Digital Visual Interface (DVI) but includes consumer electronics control (CEC). Video data is transmitted without data compression whereas audio can be transmitted with or without data compression.

The interface incorporates High-bandwidth Digital Content Protection (HDCP). High-speed data is transmitted via transition minimized differential signaling (TMDS) lines. The interface uses three TMDS lanes and one additional channel for the clock signal.

Since Version 1.4, HDMI has also supported an Ethernet data channel on the HEC lane. The display data channel (DDC), that is an I²C bus interface, is used to exchange information. Resolution compatibility is supported whenever an HDMI connection is established. Thus, extended display identification data (EDID) can be read out.

Contact assignment for connectors

Table1 lists the contact assignments for Type A connectors, which are the most commonly used connectors in TVs, monitors, DVD players and computers.

Figure 31 shows the front view of an HDMI connector. Type D micro-HDMI connectors are used for tablets, cameras and other mobile devices.

Table 17: Contact assignment for HDMI Type A connectors

Contact Type A	Signal description
Pin 1	TMDS Data2+
Pin 2	TMDS Data2 shielding
Pin 3	TMDS Data2–
Pin 4	TMDS Data1+
Pin 5	TMDS Data1 shielding
Pin 6	TMDS Data1–
Pin 7	TMDS Data0+
Pin 8	TMDS Data0 shielding
Pin 9	TMDS Data0–
Pin 10	TMDS clock+
Pin 11	TMDS clock shielding
Pin 12	TMDS clock–
Pin 13	CEC
Pin 14	reserved (HDMI1.0–1.3), HEC data– (HDMI 1.4)
Pin 15	DDC clock (I²C-Bus, SCL)
Pin 16	DDC data (I²C-Bus, SDA)
Pin 17	Ground for DDC, CEC and HEC
Pin 18	–5 V supply with 55 mA maximum current
Pin 19	Hot-Plug-Detection (all standards), HEC Data+ (HDMI 1.4)

Figure 31 | Pinout and front view of an HDMI type-A plug

HDMI key parameters and connection structure

Successive versions of HDMI standards have introduced higher data rates necessary for high-resolution displays. Table 18 shows a brief overview of HDMI versions and their maximum pixel rates, as well as maximum clock rates and TMDS bit rates. The Table also lists maximum screen resolutions for consumer applications and supported maximum color depths of the pixels. TMDS lines have a ratio between clock and bit rate of factor 10 for HDMI 1.4 and factor 14 for HDMI 2.0.

Table 18: List of key parameters for different HDMI versions

HDMI version	1.0	1.1	1.2	1.3	1.4	2.0	2.1
Maximum pixel clock rate (MHz)	165	165	165	340	340	600	no extra clock channel
Maximum TMDS bit rate per lane including 8 b/10 b coding overhead (Gbit/s)	1.65	1.65	1.65	3.4	3.4	6	12
Maximum total TMDS throughput including 8 B/10 b coding overhead (Gbit/s)	4.95	4.95	4.95	10.2	10.2	18	48
Maximum audio throughput bit rate (Mbit/s)	36.86	36.86	36.86	36.86	36.86	49.152	49.152
Maximum video resolution over 24 bit/pixel single link	1920* 1200 p/ 60 Hz	1920* 1200 p/ 60 Hz	1920* 1200 p/ 60Hz	2560* 1600 p/ 60 Hz	4096* 2160 p/ 30 Hz	4096* 2160 p/ 60 Hz	7680* 4320 p/ 60 Hz
Maximum color depth (bit/pixel)	24	24	24	48	48	48	48

Figure 32 shows the basic HDMI TMDS data connection structure of transmitters and sink connectors. The transmitter has a switched current source of 10 mA. A differential signal connection with matched impedance builds the data path to the receiver. The receiver terminates each signal line of the differential interface with 50 Ω to a 3.3 V supply line.

This leads to a single-ended nominal voltage swing (V_{SE}) of:

$$V_{SE} = 10\ mA \cdot 50\ \Omega = 500\ mV$$

Consequently, the nominal differential voltage swing is 1 V, which is twice the value of a single-ended data line. The differential nominal termination is 100 Ω, which is twice the value of the single-ended pull-up resistors of the HDMI sink connectors. The impedance matching must be kept in window between 85 Ω and 115 Ω, i.e., 100 Ω ±15%, to comply with the HDMI specification.

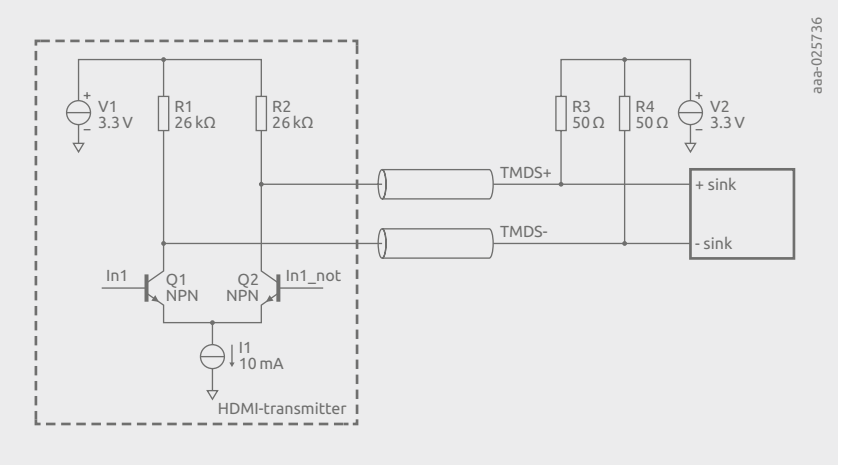

Figure 32 | Structure of an HDMI transmitter connected to a receiver

Figure 33 shows the HDMI 1.4 transmitter mask and upper and lower limits of the TMDS line voltage. The eye has a minimum height of 400 mV and a width of 0.7 unit intervals.

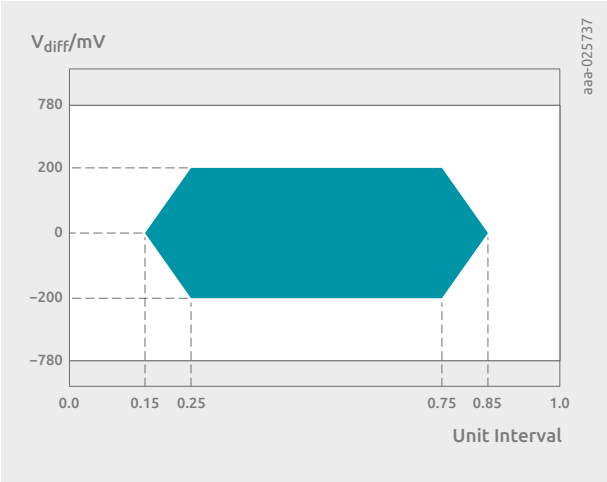

Figure 33 | Eye diagram of an HDMI transmitter 1.4 mask

Figure 34 depicts the HDMI 1.4 receiver mask. Eye height is 300 mV (±50 mV), and eye width must be at least 50% of the unit interval.

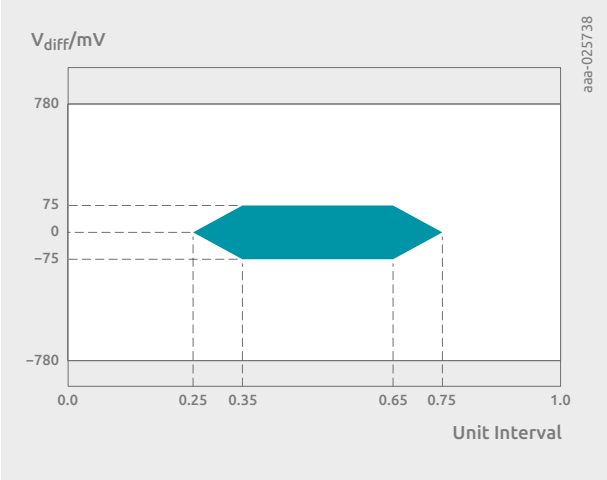

Figure 34 | Eye diagram of an HDMI transmitter 1.4 receiver side

Figure 35 shows the setup of eye diagrams for eye diagram measurements with HDMI 2.0 at the source test points. TP1 is on the pattern generator's receptacle plug, with the test point adapter (TPA). A cable emulator based on worst-case conditions is placed between TPA-P and the reference cable equalizer, followed by the TP1_EQ.

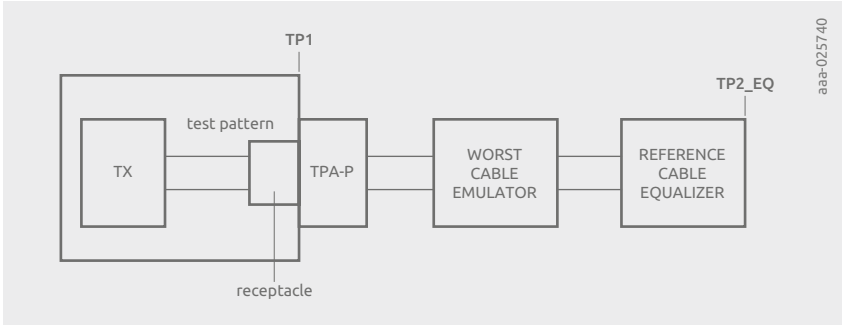

Figure 35 | HDMI source test point assignment for eye diagram measurement

Figure 36 depicts the HDMI 2.0 mask diagram for test point TP2_EQ. Eye height V and eye width H depend on the HDMI bit rate, as shown in Table 19. To achieve the maximum bit rate of 6 Gbit/s, a minimum eye height of 150 mV and the transition of the data signal must occur within the horizontal width of the mask which is defined as 0.4 of the unit interval.

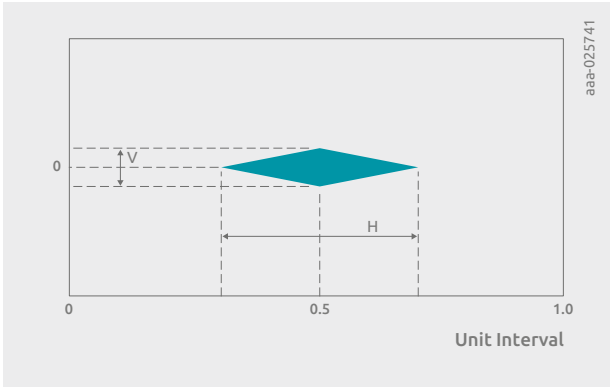

Figure 36 | HDMI2.0 mask at test point TP2_EQ for eye diagram measurements

Table 19: Mask size in dependency of the bit rate (Gbit/s)

TMDS Bit Rate (Gbit/s)	Mask width H (UI)	mask height V (mV)
3.4 < bit rate ≤ 3.712	0.6	335
3.712 < bit rate ≤ 5.94	−0.0332 * (bit rate)² + 0.2312 * (bit rate) + 0.1998	−19.66 * (bit rate)² + 106.74 * (bit rate) + 209.58
5.94 < bit rate ≤ 6.0	0.4	150

HDMI 2.1 Fixed Rate Link

With the introduction of HDMI 2.1, data transmission was upgraded to a higher level of performance level with a change from the DC-coupled TMDS interface to a new AC-coupled interface called Fixed Rate Link (FRL). Because changes had to be backward compatible for existing video receiving devices such as TVs and monitors, the topology of the transmitter was changed. On the receiver side nothing was changed.

The new FRL transmitter topology is shown in Figure 37. The output signals are coupled via a capacitor to the corresponding pins of the receiver. The transmitter now has two current sources per signal line of a lane rather than one, and both edges of the data signals are driven actively. In the TMDS transmitter only the falling edges are driven actively with a 10 mA current source. The rising edge was driven via a 50 Ω pull-up resistor. For FRL the upper current source is active and pushes current into one signal line of the lane while the other signal line of the differential pair is driven by the lower current source to low state. For the other differential logic state, the scenario is swapped for the active current sources. Figure 37 shows a Spice simulation circuit for the above-described topology. To achieve the same nominal differential swing, the current sources of the FRL transmitter operate with 5 mA. The nominal single-ended swing is 500 mV, the same as for a TMDS signal. With the AC-coupling there is the must to have DC-free signals at the transmitter because DC cannot pass a capacitor. The differential swing behind the capacitors is 1 V with the states +/– 500 mV.

The receiver side has a nominal 50 Ω termination to AV_{CC} which is 3.3V +/– 5%. AV_{CC} is the bias voltage of the inputs of the comparator in the receiver input as shown in Figure 38. In Table 20 the different HDMI versions are compared for a selection of suitable ESD protection diodes with respect to the V_{RWM} rating. With a conventional HDMI interface, the maximum voltage at the receiver cannot exceed the pull-up voltage AV_{CC}. With an FRL interface the overlaid data signal swing must be considered. For the worst-case scenario, the maximum allowed bias voltage of 3.3 V + 5% tolerance is assumed, and half of the data swing voltage is added, which is 600 mV according to the standard specification documents. For FRL signals, an extra 75 mV for the equalizing overshoots must be considered. An ESD protection diode with a V_{RWM} rating of 4 V and higher is suitable for FRL interfaces. For the latch-up risk consideration it makes no difference whether a legacy HDMI TMDS interface or updated FRL link is protected, because the bias current driving pull-up resistor connected to AV_{CC} is the same.

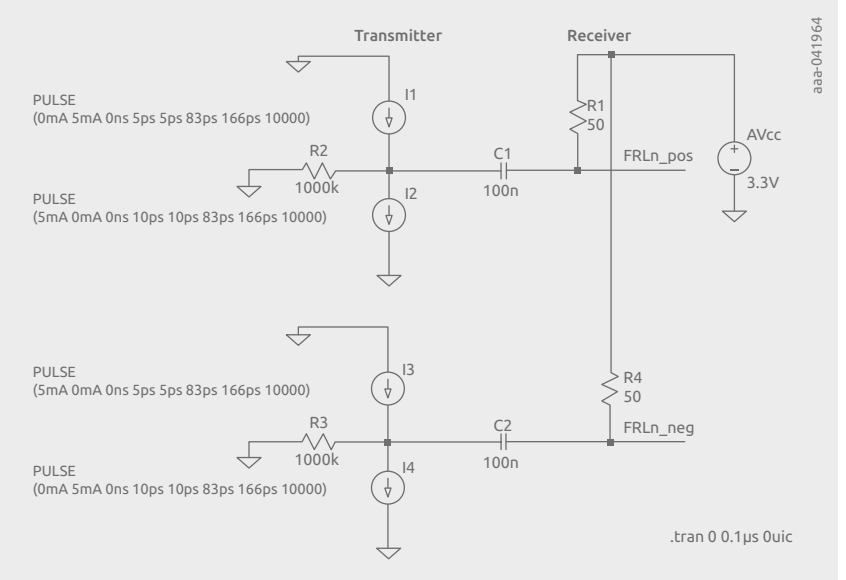

Figure 37 | Principal topology of an HDMI FRL interface

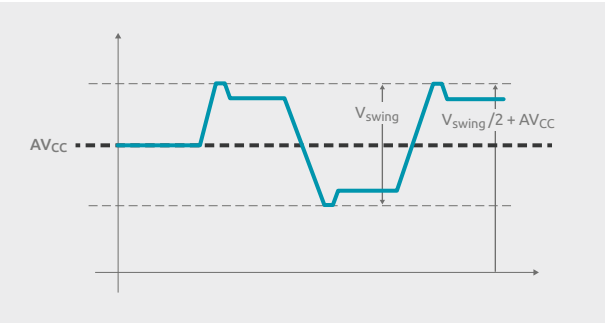

Figure 38 | Single-ended FRL input signal at a receiver input pin

Table 20: Comparison of HDMI versions for the required V_{RWM} rating of ESD protection devices.

HDMI version	Data rates	Nominal	Worst case
HDMI 1.4b	TMDS -Rate ≤ 3.4 G	3.3 V	3.465 V (+5%)
HDMI 2.1a	TMDS-3.4 < Rate ≤ 6 G	3.3 + 0.6/2 = 3.6 V*	3.465 + 0.6/2 = 3.765 V*
HDMI 2.1a	FRL 3-12G	3.3 + 0.375 = 3.675 V	3.465 + 0.375 = 3.84 V

* AC coupled source, maximum voltage swing plus AV_{CC}

7.2.2 DisplayPort

DisplayPort (DP) is a digital display interface defined by the Video Electronic Standards Association (VESA), a consortium of computing manufacturers and companies developing system chips.

The DP standard was introduced to replace not only analog video interfaces like VGA but also digital interfaces such as DVI and HDMI. As well as the video data stream, audio data is also transferred. In addition, USB data can be transmitted via an auxiliary differential channel.

DP uses packetized data transmission, which can be found in many other modern high-speed interfaces such as USB, Ethernet and PCI Express. It also uses 8B/10B coding, which allows the data clock to be regenerated from the data line signal by means of a clock-PLL. This has the advantage that no differential channel needs to be provided to transfer a dedicated clock signal. Four lanes are used for the video and audio data transmission. The AUX channel supports device management and device control data for the main link (ML). These functions are realized using the standards VESA EDID (VESA Extended Display Identification Data), DPMS (Display Power Management Signaling) and MCCS (Monitor Control Command Set).

Table 21 shows the pin assignment for the 20-pin connector at the data source side. At the sink side the ML_Lanes are placed in reverse order. This means that Lane 0 pins from the source are used for Lane 3 pins at the receiver side and that Lanes 1 and 2 are swapped.

Table 21: Pin assignment for a DP connector, source side

Pin number	Signal name	description
1	ML_Lane 0 positive	Lane 0 (+)
2	GND	Ground
3	ML_Lane 0 negative	Lane 0 (-)
4	ML_Lane 1 positive	Lane 1 (+)
5	GND	Ground
6	ML_Lane 1 negative	Lane 1 (-)
7	ML_Lane 2 positive	Lane 2 (+)
8	GND	Ground
9	ML_Lane 2 negative	Lane 2 (-)
10	ML_Lane 3 positive	Lane 3 (+)
11	GND	Ground

Pin number	Signal name	description
12	ML_Lane 3 negative	Lane 3 (-)
13	CONFIG 1	Grounded or terminated to GND
14	CONFIG 2	Grounded or terminated to GND
15	AUX Channel positive	AUX channel (+)
16	GND	Ground
17	AUX Channel negative	AUX channel (-)
18	Hot Plug	Hot plug detect
19	Return	Return for power
20	DP_PWR	Power for connector (3.3 V, 500 mA)

Since Version 1.0 of DP was released in 2006, a series of updated versions have been introduced that have increased the data rate and supported higher resolution in terms of pixels per frame, higher frame rates and greater color depth. An overview of the most important features of the different DisplayPort standards is provided in Table 22. All new standards are backwards compatible. Maximum bandwidth on one lane is 20 Gbit/s with DP 2.0/2.1a. The effective bandwidth is slightly lower because the encoding scheme introduces some redundancy for the DC balancing required. Color depth up to 16 bit resolution per color component is supported by all standards, which means that 48 bits need to be transferred per pixel for the three components that define a pixel. A pixel can be defined by the components Red, Green and Blue (RGB) or the Luminance Value Y and the Color Difference Signals CB and CR (YCB CR). RGB is transmitted with full bandwidth on each channel and referred to as 4:4:4. For YCB CR a chrominance subsampling scheme can be applied. The luminance signal is transmitted in full bandwidth because the uncolored information of a picture plays an important part in ensuring that all details are visible to the human eye. With 4:2:2, only every second pixel value is provided for the chrominance components in a line on the display and with 4:2:0 the vertical resolution is reduced by a factor of 0.5. Two lines then have identical color information.

Table 22: List of most important features for the different DP versions

	DisplayPort version				
	1.0/1.1a	1.2/1.2a	1.3	1.1/1.4a	2.0/2.1a
ML Main link					
Number of lanes	4	4	4	4	4
Maximum total bandwidth (all lanes) in Gbit/s	10.8	21.6	32.4	32.4	80
Maximum total data rate	8.64	17.28	25.92	25.92	77.37
Encoding scheme	8b/10b	8b/10b	8b/10b	8b/10b	128b/132b
Color space support					
ITU-R BT.601	x	x	x	x	x
ITU-R BT.709	x	x	x	x	x
sRGB	–	x	x	x	x
scRGB	–	x	x	x	x
xvYCC	–	x	x	x	x
Adobe RGB (1998)	–	x	x	x	x
DCI-PC3	–	x	x	x	x
Simplified color profile	–	–	x	x	x

In Figure 39 the topology of a main link differential data pair is shown. There is an AC-coupling at the TX-side and a 50 Ω termination to a bias voltage $V_{bias\text{-}TX}$ at the transmitter side and $V_{bias\text{-}RX}$ for the receiver side of the lane. The bias voltage can be in a range from 0 V to 2 V. The AC coupling is a major difference from an HDMI interface, which has a DC-connection and a pull-up voltage of 3.3 V nominal.

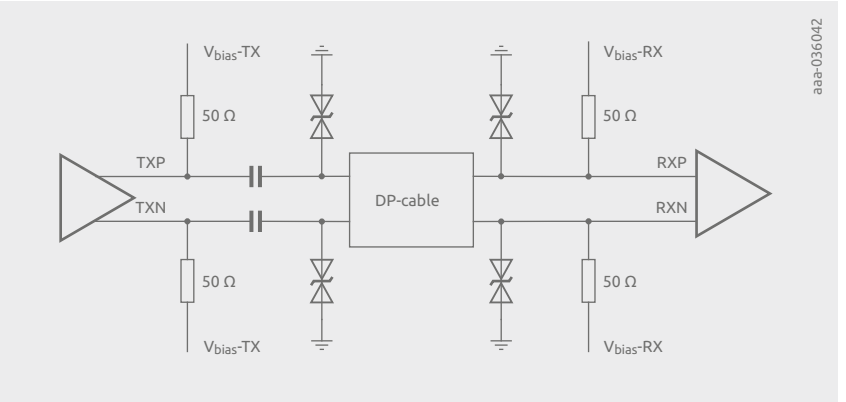

Figure 39 | Structure of a Main Link (ML) lane for DP

7.3 MIPI interface

The MIPI Alliance comprises several companies that define a data communication standard for interfacing processor and chip sets to peripheral components such as cameras, sensors and displays. Application areas include mobile devices like smartphones and tablets, and embedded systems like TVs. In automotive, MIPI is commonly used for camera applications. However, many of the MIPI specifications are already used or adapted for automotive applications.

Although most MIPI interfaces are not normally used for external interfaces with direct access for users, ESD protection is applied to safeguard against ESD strikes entering a device via housing gaps or in case of an opened cover. Key facts regarding the physical layer of MIPI standards D-PHY, M-PHY and C-PHY are discussed in subsequent chapters of this guide. The recently announced A-PHY specification is described briefly in Section 7.6.5 as it is a SerDes interface.

7.3.1 MIPI D-PHY

MIPI D-PHY is a synchronous connection between a master and slave, and the master provides the clock signal as a unidirectional signal. One or more data lanes can be used for data transmission. The minimum configuration consists of two differential signal connections or lanes - one clock lane and at least one data lane. The direction of data flow can be unidirectional and bidirectional. Data flow direction is indicated by an exchange of tokens in half-duplex mode. The data speed in reverse direction is a fourth of forward direction.

A low-voltage level signal is transmitted in high-speed mode, transferring data in a burst mode. A so-called low-power signaling mode is used for transmission of control commands. The specification does not mention a fixed maximum data rate per lane, but indicates a range from 80 Mbit/s to 1500 Mbit/s. If a higher data rate is required, the number of differential data pairs must be increased.

Figure 40 shows an example for the line levels on a signal line of MIPI D-PHY. The red part of the signal shows a high-speed data burst, whereas the blue part shows a low-power signaling event.

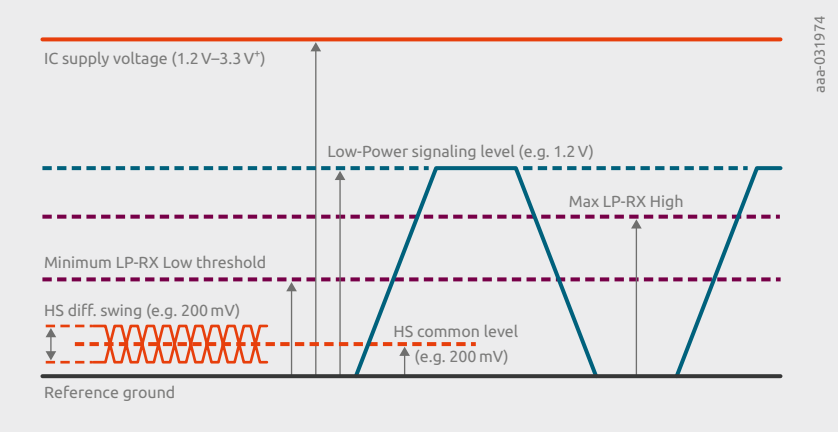

Figure 40 | Line levels for MIPI D-PHY

The lane states are listed in Table 23. A data lane can operate in either high-speed mode or low-power mode. High-speed data transmission starts and stops with stop state LP-11, which is a single-ended high-state on both lines of the differential pair.

The sequence to be sent for high-speed operation is LP-11 (stop), LP-01 (high-speed request), LP-00 (bridge), and the interface remains in high-speed mode until a stop command is received. The control mode is the default condition of the interface, while escape modes can be entered via a request sent in control mode.

Table 23: Lane states for MIPI D-PHY

State Code	Line Voltage Levels		High-Speed	Low Power	
	Dp-Line	Dn-Line	Burst Mode	Control Mode	Escape Mode
HS-0	HS Low	HS High	Differential-0	not applicable	not applicable
HS-1	HS High	HS Low	Differential-1	not applicable	not applicable
LP-00	LP Low	LP Low	not applicable	Bridge	Space
LP-01	LP Low	LP High	not applicable	HS-Request	Mark-0
LP-10	LP High	LP Low	not applicable	LS-Request	Mark-1
LP-11	LP High	LP High	not applicable	Stop	not applicable

On the transmitter side, the maximum output voltage in high state V_{OH} in low-power Mode is 1.3 V, while the minimum level for the low state V_{OL} is −50 mV as shown in Table 24.

Table 24: Transmitter DC characteristics for low-power mode

Parameter	Description	min	nominal	max
V_{OH}	output level high-state	1.1 V	1.2 V	1.3 V
V_{OL}	output level low-state	−50 mV	0 mV	50 mV

On the receiver side, the minimum input voltage in logical high-state V_{IH} in low-power Mode is 880 mV. The input level for the logical low state must stay below 300 mV, as Table 25 shows.

Table 25: Receiver DC characteristics for low-power mode

Parameter	Description	min	nominal	max
V_{IH}	input level high-state	880 mV	–	–
V_{IL}	input level low-state	–	–	300 mV

Table 26 lists the most important transmitter DC characteristics. The differential lines have a nominal common mode voltage of 200 mV overlaid with the HS signal of 100 mV single-ended swing, which means 200 mV nominal differential swing amplitude.

Table 26: High-speed transmitter DC characteristics

Parameter	Description	min	nominal	max
V_{CMTX}	HS transmitter static common mode voltage	150 mV	200 mV	250 mV
$\|V_{DD}\|$	HS transmitter differential voltage	140 mV	200 mV	270 mV
V_{OHHS}	HS output high-level voltage	–	–	360 mV
Z_{OS}	single ended output resistance	40 Ω	50 Ω	62.5 Ω
ΔZ_{OS}	single ended output resistance mismatch	–	–	10%

On the receiver side, at least +/– 70 mV are required to exceed the thresholds for the differential voltage for logical high or low state as shown in Table 27.

Table 27: High-speed receiver DC characteristics

Parameter	Description	min	nominal	max
V_{CMRX}	Common mode voltage HS receive mode	70 mV	–	330 mV
V_{IDTH}	Differential input high state threshold	–	–	70 mV
V_{IDTL}	Differential input low state threshold	–70 mV	–	–
V_{IHHS}	Single-ended input high voltage	–	–	460 mV
V_{ILHS}	Single-ended input low voltage	–40 mV	–	–
Z_{ID}	Differential input impedance	80 Ω	100 Ω	125 Ω

7.3.2 MIPI M-PHY

MIPI M-PHY is the successor of the MIPI D-PHY standard. It addresses the growing demand for higher data rates per lane, better power efficiency and greater flexibility. It uses a synchronous connection between a master and slave. The clock signal is generated via a clock PLL, so there is no dedicated clock signal transmitted from a master as with D-PHY interfaces.

Figure 41 shows an example of a MIPI M-PHY interface in which unidirectional lanes are used as data connections. Every lane connects an M-TX transmitter block to an MN-RX receiver block. For higher data rates, several lanes can be used in both directions.

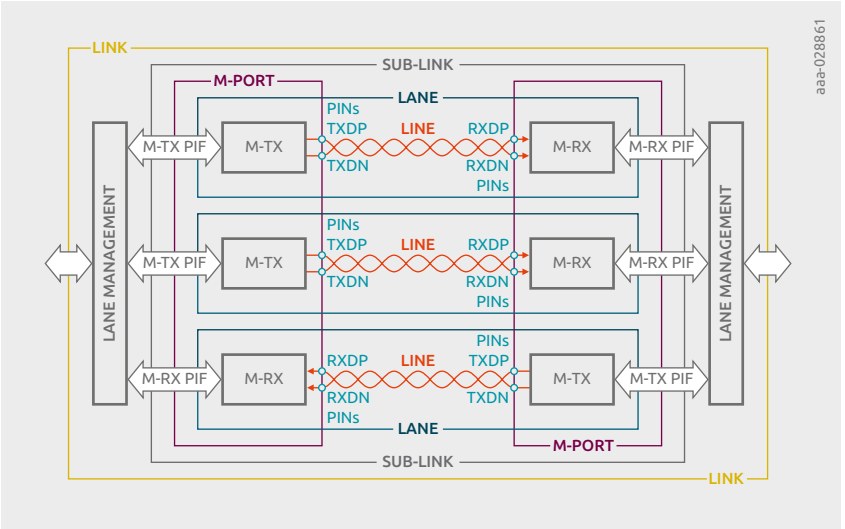

Figure 41 | MIPI M-PHY example for the lane structure

Data is transmitted in the so-called HS-burst state in HS-mode encoded in 8b10b and put on the signal lines in non-return-to-zero (NRZ) signaling. There are two series defined with related data rates that are denoted as a GEAR for each couple. The different supported data rates are listed in Table 28.

Table 28: High-speed burst data rate, M-PHY series and GEARs

Rate A-series (Mbit/s)	Rate B-Series (Mbit/s)	High-Speed GEARs
1248	1457.6	HS-G1 (A/B)
2496	2915.2	HS-G2 (A/B)
4992	5830.4	HS-G3 (A/B)
9984	11680.8	HS-G4 (A/B)

Figure 42 shows the termination scheme of MIPI M-PHY. The TX drivers switch one of the differential lines to ground and the other line to V_{LD} depending on the differential lane state. Each driver output has a serial resistor R_{SE_TX} connected to the outgoing signal line. 40 Ω is the minimum value for R_{SE_TX}, the maximum allowed value is 60 Ω. The receiver side RX only requires a termination in the high-speed mode.

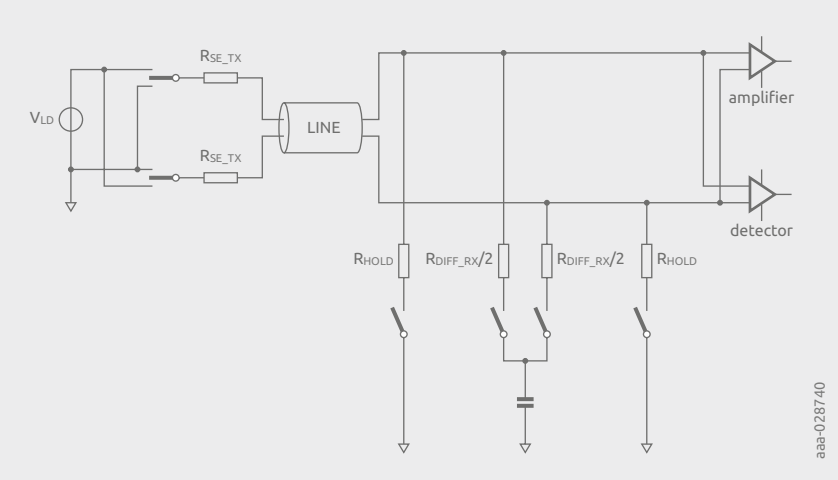

Figure 42 | MIPI M-PHY termination scheme (repair the typo in the picture "amplifier" not ampliier

Figure 43 shows the transmitter side MIPI M-PHY eye diagram for the high-speed mode in GEAR 3 and GEAR 4. The minimum eye height is 80 mV. The temporal eye width must be 0.55 unit intervals in GEAR 3 and 0.5 unit intervals in GEAR 4. These key parameters are listed in Table 29.

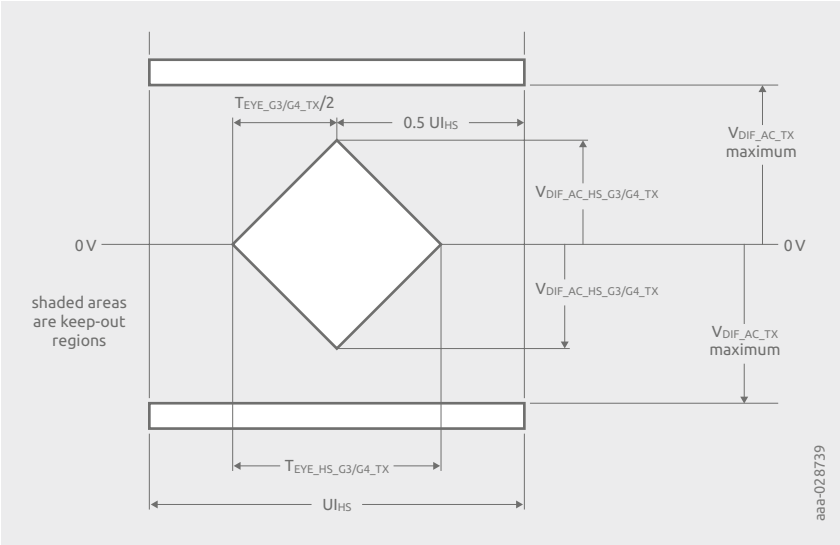

Figure 43 | M-PHY TX mask for HS-mode GEAR 3 and GEAR 4

Table 29: High-speed GEAR 3 and GEAR 4 electrical key parameters for TX (transmitter side)

Parameter	Value	Description
$V_{DIF\_AC\_HS\_G3/4\_TX}$	40 mV, minimum	Differential TX AC voltage in HS-G3/4
$V_{DIF\_AC\_HS\_G4\_TX}$	40 mV, minimum	Differential TX AC voltage in HS-G4
$T_{EYE\_HS\_G3\_TX}$	0.55 Unit intervals (UI)	Transmitter eye opening in HS-G3
$T_{EYE\_HS\_G4\_TX}$	0.5 Unit intervals (UI)	Transmitter eye opening in HS-G4

The receiver-side eye diagram looks like the transmitter-side diagram. For the highest data speed of MIPI M-PHY high-speed GEAR 4, the height of the eye is the same as the transmitter eye height. It is twice $V_{DIF\_AC\_HS}$, equal to 40 mV as minimum requirement. The open eye width $T_{EYE\_HS\_G4\_RX}$ is defined as 1 – TJRX measured in unit intervals. TJRX is lower or equal to 0.52 unit intervals for GEAR 4. This means that the open eye is 0.48 unit intervals wide in temporal direction as a minimum requirement.

7.3.3 MIPI C-PHY

MIPI C-PHY uses three signal lines instead of two lines for conventional differential data lanes. This allows a higher data rate without needing four signal lines for two parallel standard differential lanes. MIPI C-PHY achieves 2.28 bits per symbol. It has some similarities with MIPI D-PHY for the transition between low-power modes and high-speed modes. Unlike the D-PHY standard, no separate clock channel is provided. The combination of signal voltages on the signal lines changes from symbol to symbol. This makes it comparatively simple to regenerate the clock signal because of transitions after each symbol.

The maximum symbol rate is 3 GSps (Giga Symbols per second). This symbol rate is the relevant value for the frequency spectrum to be considered for the selection of ESD protection devices. 1.5 GHz is the highest frequency of the fundamental wave in high-speed mode.

Table 30 shows the signal voltages for the signal lines A, B and C in the columns wire amplitude, the receiver differential input voltages A-B, B-C and C-A, and the related digital output stages. The line voltages are all combinations of 0.25 V, 0.5 V and 0.75 V for the three wires. The corresponding three voltage differences have a sum of zero for every state +x, –x, +y, –y, +z or –z. A positive difference corresponds to a digital high state for the digital output of the receiver.

Table 30: Signal voltages and differential voltages for the six MIPI C-PHY lane states

Wire State	Wire Amplitude			Receiver differential input voltage			Receiver digital output		
	A	B	C	A-B	B-C	C-A	Rx-AB	RX-BC	RX-CA
+x	3/4 V	1/4 V	1/2 V	+1/2 V	–1/4 V	–1/4 V	1	0	0
–x	1/4 V	3/4 V	1/2 V	–1/2 V	+1/4 V	+1/4 V	0	1	1
+y	1/2 V	3/4 V	1/4 V	–1/4 V	+1/2 V	–1/4 V	0	1	0
–y	1/2 V	1/4 V	3/4 V	+1/4 V	–1/2 V	+1/4 V	1	0	1
+z	1/4 V	1/2 V	3/4 V	–1/4 V	–1/4 V	+1/2 V	0	0	1
–z	3/4 V	1/2 V	1/4 V	+1/4 V	+1/4 V	–1/2 V	1	1	0

Figure 44 shows how the six lane states are realized to achieve the voltages for the signal lines according to Table 31 . At the transmitter side the lines can be switched to the driver voltage V+ or ground via a 50 Ω termination via a pull-up (PU) or pull-down (PD) switching FET. Together with the receiver termination of 2 × 50 Ω between the two comparator inputs, the voltage levels +/– 1/4 V and +/– 3/4 V are generated. For example, in the line state +x, the driver voltage +V is switched to the A line via a 50 Ω resistor by the switch PU_A. The positive input of the comparator RX_AB is connected to a divider created by this 50 Ω PU and the 100 Ω between the comparator inputs plus the PD resistor of 50 Ω from the switch PD_B connected to ground. This results in the 3/4 +V level on the A signal wire. A second stage with 100 Ω PU and PD resistors and switching FETs creates the 1/2 +V voltage for a signal line. This can be seen, for example, in state +x for the C signal wire.

If +V is connected to line A (via PU_A) and the switch to ground is active at line B (PD_B), the state +x is called A to B as well. For the opposite polarities, the state –x can be nominated B to A. The corresponding receiver, RX_AB in the example discussed, the receiver difference is either +1/2 +V or –1/2 +V. This is the background for so-called positive or negative polarity like the left and right separation in Figure 44. For the second row with the two y states the same system can be applied for the wires B and C and the polarity is reflected in the polarity of the differences at the inputs of RX_BC.

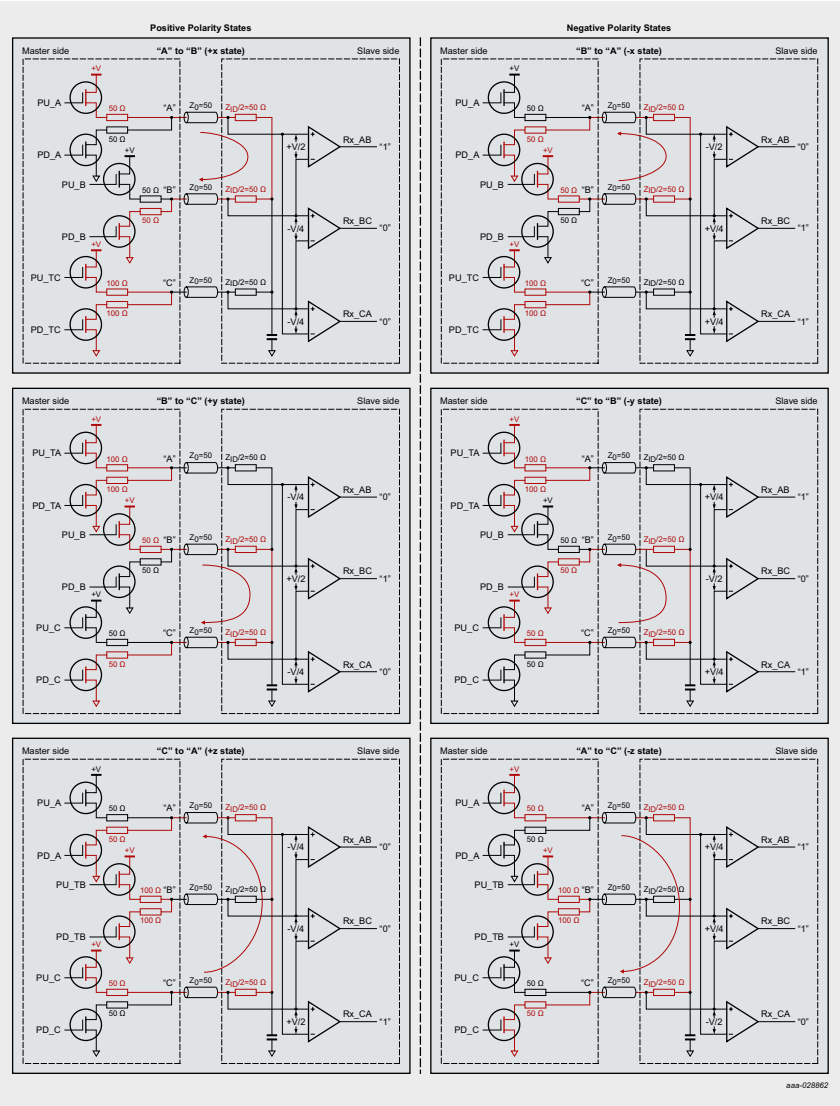

Figure 44 | The six C-PHY wire states in nominal condition, with driver and receiver-side structures

For each of the six possible states, there are five possible transitions to any other state. These transitions are depicted in Figure 45. As in Figure 44 the states are divided into positive and negative polarities in the inner circle and the negative states outside the inner circle.

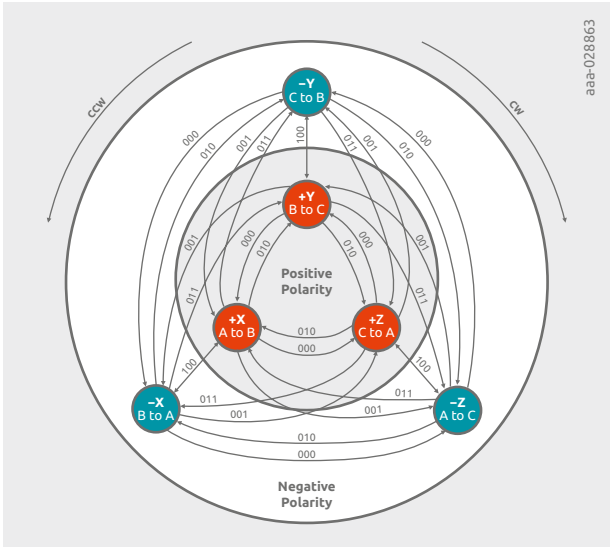

Figure 45 | All six MIPI C-PHY states with all five possible transitions

Each transmitted symbol is represented by a three-bit number for the transitions between the six wire states with the values 000, 001, 010, 011 and 100. These values are shown in blue at the transition arrows. C-PHY defines three state change parameters - flip, rotate and polarity - represented in the three bits of the transition values.

The least significant bit indicates a polarity change, shown by a change from light grey area to dark grey or in the opposite direction in the diagram. The next significant bit indicates the direction of rotation in the diagram for the wire state. If it is clockwise (CW in diagram) the bit is set to 1, in the counterclockwise direction (CCW) it is 0.

Finally, the most significant bit stands for a flip of the same state in polarity. This is, for example, a change from state +x to –x or vice versa. Flip transitions are represented with the value 100. Polarity changes and rotation bits are put to zero.

Table 31 shows all five transitions with the symbol values in the left-hand column from every wire state in time interval N-1 to any other present state. The right-hand column indicates which facts can be assigned to each transition in direction of rotation and polarity change, and the flip case, indicated also as same phase in the C-PHY standard.

Table 31: Transitions from previous state to present state

Symbol Input Value	Previous Wire state, interval N-1						description of transition facts
	+x	−x	+y	−y	+z	−z	
000	+z	−z	+x	−x	+y	−y	Rotate CCW, pol. is the same
001	−z	+z	−x	+x	−y	+y	Rotate CCW, pol. is opposite
010	+y	−y	+z	−z	+x	−x	Rotate CW, pol. is the same
011	−y	+y	−z	+z	−x	+x	Rotate CW, pol. is opposite
1xx	−x	+x	−y	+y	−z	+z	same phase, pol. is opposite

Figure 46 shows a receiver eye diagram for MIPI C-PHY in high-speed mode. The eye's height must be at least 80 mV, twice V_{IDTH} threshold voltages for the differential receivers. The eye width $T_{EYE\_WIDTH\_RX}$ is at least 0.5 unit intervals.

The maximum signal voltage on a line can be 1.35 V, which is related to LP mode.

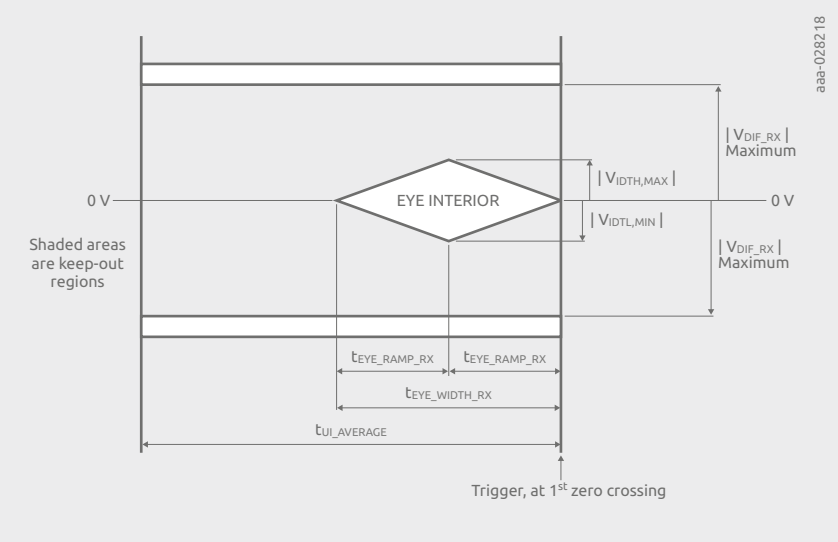

Figure 46 | High-speed mode receiver mask for MIPI C-PHY

Figure 47 gives an example of an eye measurement at a C-PHY interface. The signal shows the voltage levels 'Strong 0' and 'Strong 1' as well as 'Weak 0' and 'Weak 1' as is be expected from Table 30. The test scope is triggered at the right side zero crossing behind the open eye.

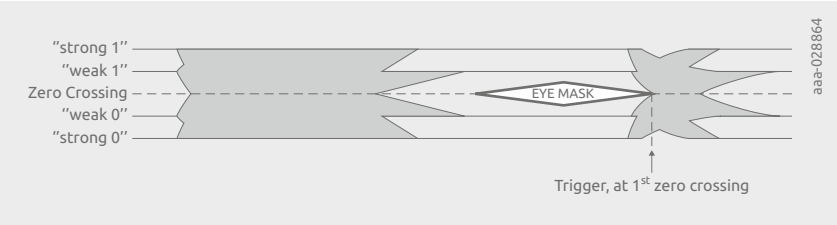

Figure 47 | Eye diagram mask for MIPI C-PHY

7.4 PCIe interface

The abbreviation PCIe stands for Peripheral Components Interconnection Express,a high-speed serial data interface introduced in 2003 by a consortium of Intel, Dell, HP and IBM. It replaced slower interfaces such as PCI, PCI-X and AGP, and is the standard for connecting peripheral components like graphic cards, SSDs, sound cards or any data-capture cards with the main processor chipset in computing devices. It supports full duplex communication between any two endpoints and its protocol is used as the base for other high-speed interfaces such as SATA Express, M.2, U.2 and Thunderbolt. Its principles also underpin fast memory card interfaces like CFexpress and SD Express.

A lane for a PCIe interface consists of two differential pairs, one for receiving data and the other for transmitting data. The number of lanes can vary from one up to 16 and is indicated using an 'x' prefix, so 'x16' represents the largest standard implementation for PCIe data buses.

For Versions 1.0/1.1 to 2.0/2.1 of PCIe, data is encoded with 8b/10b. Versions 3.0/3.1 to 5 use a 128b/130b encoder. Encoders ensure that the data signal is DC-free, i.e. that the number of 1/0 logic states is identical on average. This is important because a capacitor in the range from 75 nF to 220 nF must be placed at the transmitter side of each data line. (This AC-coupling is familiar from the RX/TX lines in USB interfaces.) PCIe Versions 6.0 and 7.0 introduced PAM-4 coding (pulse amplitude modulation with four logic-states) and forward error correction (FEC). Every symbol can transfer 2-bit content. PCIe does not provide a separate clock channel but the clock signal is recovered from the serial data signals.

Table 32: Key data transfer characteristics of PCIe versions

PCIe Version	1.0/1.1	2.0/2.1	3.0/3.1	4.0	5.0	6.0	7.0
Maximum transfer rate in Tranfers/s	2.5 GT/s	5 GT/s	8 GT/s	16 GT/s	32 GT/s	32 GT/s	64 GT/s
Line Code	NRZ, 8b/10b Running Disparity (RD)		NRZ, 128b/130b			PAM-4 CRC and FEC FLIT 242/256	
Bits per transfer	0.8		128/130 ~ 0.985			(242/256)*2 ~ 1.9	
Lanes	**Data Throughput (encoded serial bit rate) in GB/s**						
x1	0.25	0.5	0.985	1.969	3.938	7.563	15.125
x2	0.5	1	1.969	3.938	7.877	15.125	30.25
x4	1	2	3.938	7.877	15.754	30.25	60.5
x8	2	4	7.877	15.754	31.508	60.5	121
x16	4	8	15.754	31.508	63.015	121	242

Table 32 shows a list of key characteristics with respect to data transfer rates for different versions of PCIe, ranging from the minimal one-lane (x1) interface up to 16 lanes (x16). Table 33 shows the pin assignment of the connectors for x1, x4, x8 and x16. The signal pin PRSNT1# needs to be connected to a PRSNT2# pin at the longest distance on a PCB. With this approach the number of lanes can easily be detected.

The PCIe interface uses two supply voltages of 12 V and 3.3 V. For the 3.3 V supply, a load of up to 3 A is allowed for all PCIe cards. For x16, cards up to 5.5 A can be supported from

12 V which is power of 66 W. Up to 75 W can be supported after a card has been initialized and recognized as a high-power device.

When selecting ESD protection devices, the following factors are important regarding the standoff voltage V_{RWM}. The common mode voltage at the receiver pins can vary from 0.7 V up to 1.2 V. Typically, 0.9 V to 1 V are implemented. The single-ended peak-to-peak voltage swing is typically 0.8 V. The data signal changes with +/– 400 mV against the common mode voltage.

An ESD-diode should have a V_{RWM} of at least 1.6 V (1.2 v plus 0.4 V).

Table 33: Pin assignment for PCIe x1, x4, x8 and x16

Pin	Side B	Side A	Description
1	+12 V	PRSNT1#	PRSNT1# must be connected to farthest PRSNT2# pin
2	+12 V	+12 V	Main power pins
3	+12 V	+12 V	
4	Ground	Ground	
5	SMCLK	TCK	SMBus and JTAG port pins
6	SMDAT	TDI	
7	Ground	TDO	
8	+3.3 V	TMS	
9	TRST#	+3.3 V	
10	+3.3 V aux	+3.3 V	Aux power and Standby power
11	WAKE#	PERST#	Link reactiivation, fundamental reset
Key notch			
12	CLKREQ#	Ground	Clock request signal
13	Ground	REFCLK+	Reference clock, differential pair
14	HSOp(0)	REFCLK–	Lane 0 transmit data, + and –
15	HSOn(0)	Ground	
16	Ground	HSIp(0)	Lane 0 receive data, + and –
17	PRSNT2#	HSIn(0)	
18	Ground	Ground	
PCI Express x1 cards end at pin 18			
19	HSOp(1)	Reserved	Lane 1 transmit data, + and –
20	HSOn(1)	Ground	
21	Ground	HSIp(1)	Lane 1 receive data, + and –
22	Ground	HSIn(1)	
23	HSOp(2)	Ground	Lane 2 transmit data, + and –
24	HSOn(2)	Ground	
25	Ground	HSIp(2)	Lane 2 receive data, + and –
26	Ground	HSIn(2)	
27	HSOp(3)	Ground	Lane 3 transmit data, + and –
28	HSOn(3)	Ground	
29	Ground	HSIp(3)	"Lane 3 receive data, + and –, Power Brake, active low to reduce device power"
30	PWRBRK#	HSIn(3)	
31	PRSNT2#	Ground	
32	Ground	Reserved	
PCI Express x4 cards end at pin 32			
33	HSOp(4)	Reserved	Lane 4 transmit data, + and –
34	HSOn(4)	Ground	
35	Ground	HSIp(4)	Lane 4 receive data, + and –
36	Ground	HSIn(4)	
37	HSOp(5)	Ground	Lane 5 transmit data, + and –
38	HSOn(5)	Ground	
39	Ground	HSIp(5)	Lane 5 receive data, + and –
40	Ground	HSIn(5)	
41	HSOp(6)	Ground	Lane 6 transmit data, + and –
42	HSOn(6)	Ground	
43	Ground	HSIp(6)	Lane 6 receive data, + and –
44	Ground	HSIn(6)	
45	HSOp(7)	Ground	Lane 7 transmit data, + and –
46	HSOn(7)	Ground	
47	Ground	HSIp(7)	Lane 7 receive data, + and –
48	PRSNT2#	HSIn(7)	
49	Ground	Ground	
PCI Express x8 cards end at pin 49			
50	HSOp(8)	Reserved	Lane 8 transmit data, + and –
51	HSOn(8)	Ground	
52	Ground	HSIp(8)	Lane 8 receive data, + and –
53	Ground	HSIn(8)	
54	HSOp(9)	Ground	Lane 9 transmit data, + and –
55	HSOn(9)	Ground	
56	Ground	HSIp(9)	Lane 9 receive data, + and –
57	Ground	HSIn(9)	
58	HSOp(10)	Ground	Lane 10 transmit data, + and –
59	HSOn(10)	Ground	
60	Ground	HSIp(10)	Lane 10 receive data, + and –
61	Ground	HSIn(10)	
62	HSOp(11)	Ground	Lane 11 transmit data, + and –
63	HSOn(11)	Ground	
64	Ground	HSIp(11)	Lane 11 receive data, + and –
65	Ground	HSIn(11)	
66	HSOp(12)	Ground	Lane 12 transmit data, + and –
67	HSOn(12)	Ground	
68	Ground	HSIp(12)	Lane 12 receive data, + and –
69	Ground	HSIn(12)	
70	HSOp(13)	Ground	Lane 13 transmit data, + and –
71	HSOn(13)	Ground	
72	Ground	HSIp(13)	Lane 13 receive data, + and –
73	Ground	HSIn(13)	
74	HSOp(14)	Ground	Lane 14 transmit data, + and –
75	HSOn(14)	Ground	
76	Ground	HSIp(14)	Lane 14 receive data, + and –
77	Ground	HSIn(14)	
78	HSOp(15)	Ground	Lane 15 transmit data, + and –
79	HSOn(15)	Ground	
80	Ground	HSIp(15)	Lane 15 receive data, + and –
81	PRSNT2#	HSIn(15)	
82	Reserved	Ground	

Legend

Ground Pin	Zero voltage reference
Power Pin	supply power to the PCIe card
Sense pin	pins connected on card
Open drain	may be pulled low or sensed by mukltiple cards
Card-to-host pin	signal from the card to the motherboard
Host-to-card pin	signal from the motherboard to the card
Reserved	not presently used, do not connect

7.5 Ethernet

7.5.1 Ethernet standards

Ethernet is a computer network technology that is widely used in all consumer and industrial markets. It was introduced in 1980 and standardized by the IEEE in 1983. Since then, there have been a large number of different standards within 803.2, covering different markets, data rates and specific applications. Table 34 shows a selection of standards. Most Ethernet standards are aimed at consumer or industrial markets and have a major impact on industrialization or home applications such as local area networks (LAN). These networks need to transmit data over distances of several hundred meters. In most cases, differential transmission is used due to its robustness. Depending on the data rate of the respective standard, unshielded or shielded twisted pair cables are used. The nomenclature of the standard usually includes the data rate, the type of transmission and the number of lines, for example 100Base-T1 has data rate of 100Mbps, 'T' stands for twisted pair, and '1' is the line coding.

Table 34: Selection of Ethernet standards for industrial and automotive markets

Standard (IEEE)	Name	Speed	Target market	Release date
802.3	10Base5	10 Mbps	Consumer	1983
802.3	10Base2	10 Mbps	Consumer	1985
802.3i	10Base-T	10 Mbps	Consumer / Industrial	1990
802.3u	100Base-TX	100 Mbps	Consumer / Industrial	1995
802.3ab	1000Base-T	1 Gbps	Consumer / Industrial	1999
802.3an	10GBase-T	10 Gbps	Consumer	2006
802.3da	10Base-T1S	10 Mbps	Automotive	(TBD)
802.3bw	100Base-T1	100 Mbps	Automotive	2015
802.3bp	1000Base-T1	1 Gbps	Automotive / Industrial	2016
802.3ch	MGBase-T1	2.5/5/10 Gbps	Automotive	2020
802.3cy	MGBase-T1	> 10Gbps	Automotive	(TBD)

Today, Ethernet interfaces are popular in all market segments and application areas. Ethernet has become an important part of the Internet infrastructure and is used in industrial and private networks. This is mainly due to its flexibility and the IP-based communication protocol.

Ethernet communication usually works with differential transmission, which is supported by twisted pair cables (UTP). Differential transmission is much more stable, less sensitive to external interference and offers lower electromagnetic emission compared to one-way transmission. However, the type and complexity of the UTP cable are strongly related to the data rate of the Ethernet standard. Generally, UTPs are used for applications up to 1000 Mbps. These cable types are cheap, easy to implement and have sufficient bandwidth for signal transmission. However, for Ethernet standards above 1000Mbps, shielded cables are used to meet signal integrity requirements (see Figure 48). The maximum cable length typically goes up to 100 m or 200 m, which introduces some additional challenges.

1. Even in a carefully designed harness, there is a significant risk when coupling a significant amount of energy onto the Ethernet cables due to partial coupling of lightning strikes, power cables or any other external electromagnetic sources. In particular, due to the long cables the risk of coupling an significant amount of energy is increased which might lead to destructive failures [6], [7], [8].

2. Cable discharge events may happen when a pre-charged cable is plugged into a PCB connector. This is general issue for all wired interfaces. However, the impact is much more increased when it comes to long cables [9].

This leads to some series ESD and especially surge requirements of Ethernet which are described in IEC61000-4-4 (burst), IEC61000-4-5 (8/29 µs surge) and IEC60060-1 (10/700 µs surge). When it comes to protection, a suitable ESD protection device capable of clamping surge pulses is needed. The surge capability is given by the I_{ppm} value in the datasheet. This value is always related to a dedicated surge pulse. In general, there are two positions of the ESD device on the PCB (see Figure 49), which also depends on the selection of other components such as magnetics. The choice of the ESD device on the PHY side requires careful consideration of the on-chip ESD of the PHY to ensure the eternal ESD device shows a lower voltage characteristic providing a lower impedance path for the ESD pulse. Usually, an ESD device with 5 V0 down to 2 V is used here. In the second position of the ESD device between the magnetics higher voltage ESD device can also be used. This is due to the fact that the CMC with its inductance in the range of ~100uH blocks the current into the PHY when a very fast transient such as an ESD pulse is applied and gives the ESD device some time to be activated and to clamp the ESD current. In real life application, this can give some additional robustness to the interface and is the preferred position for the ESD protection.

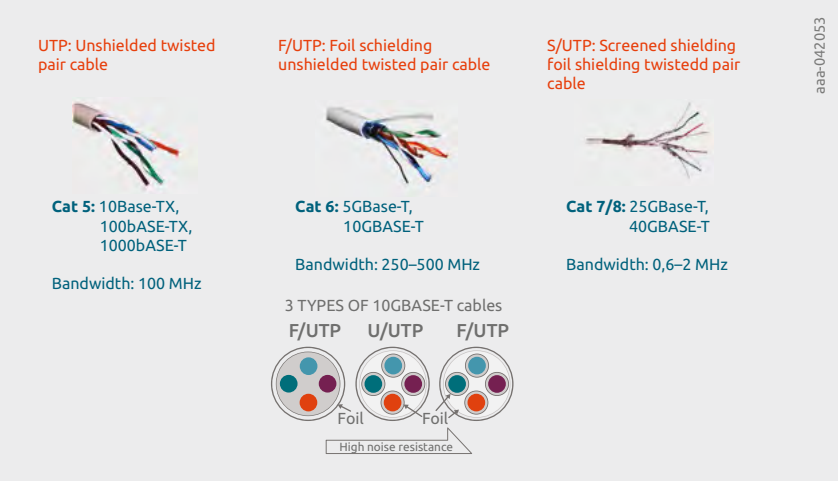

Figure 48 | Cable types used for Ethernet interfaces

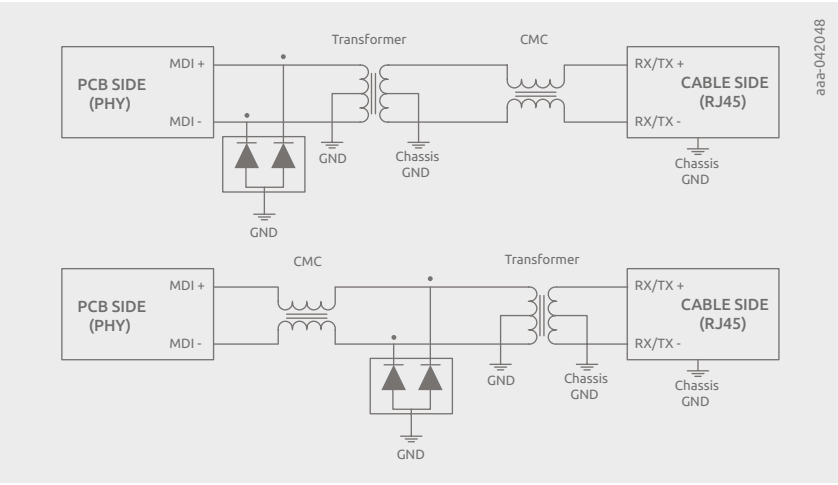

Figure 49 | Schematic of a typical Ethernet PCB including the main components, magnetics and the ESD protection device. In general, there are two different placements of ESD possible, on the PHY side and between the CMC and the transformer.

7.5.2 Power over Ethernet (PoE)

Power over Ethernet (PoE) and power over data line (PoDL), also called single-pair power over Ethernet (SPoDL), all describe several standards (802.3bu) which provide electric power along with data over a twisted pair. There is also an option for single-ended transmission called power over coax (PoC) (see Figure 50). There are different options for how much power can be transferred over the different standards, as shown in Table 35. Up to 48 V can be transferred via PoDL and PoC, which includes all relevant battery voltages (12 V, 24 V and 48 V) and allows a broad range of usage for these standards.

However, the use of any of these power delivery options has an impact on the ESD protection strategy.

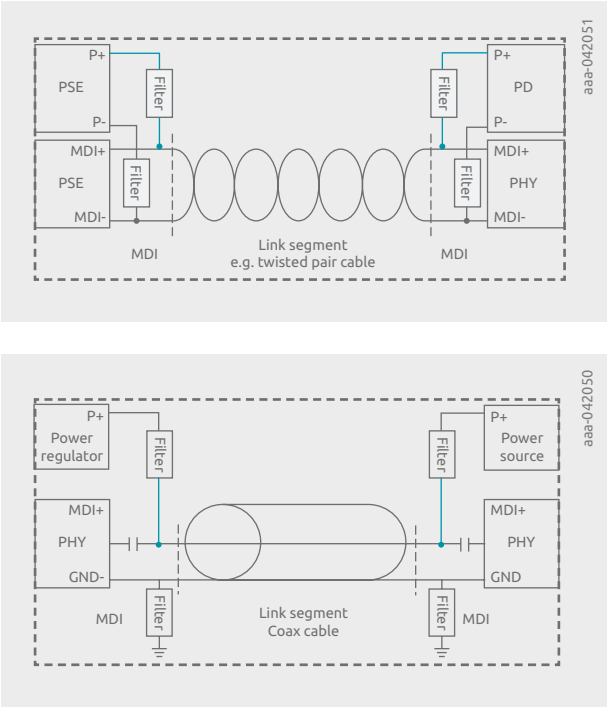

Figure 50 | Block diagram for a single-pair PoDL (left) and PoC below. PSE = power sourcing equipment, PD = powered device.

Table 35: Overview of different power delivery standards

	Power over Ethernet (PoE)	Power over Data Line (PoDL)	Power over Coax (PoC)
Standard	802.3 Clausse 33	802.3 bu	Standard adopted to 802.3 bu
Power	Max. 25 W (100 W)	16 power classes, up to 65.3 W	
Voltage	57 V	Up to 48 V	Up to 48 V
Current	Current limits	Current limited by cable, connector inductors	Current limited by cable, connector inductors
Power coupling	Transformer	Inductor	Inductor

The placement and the voltage rating of the ESD device should be considered in detail. From the protection point of view, the ESD device should be placed as close to the connector as possible. The voltage of the power delivery is then on the same net, as depicted in Figure 51. This requires an ESD device with a voltage rating higher than the voltage V_b delivered over the data lines. In detail it means that:

- the stand-off voltage V_{RWM} should be higher than the operation voltage and V_b because of leakage and possible degradations:
- the trigger voltage V_t should be higher than V_b to not activate the ESD device:
- the holding voltage V_h should be higher than V_b b to mitigate the risk of latch-up.

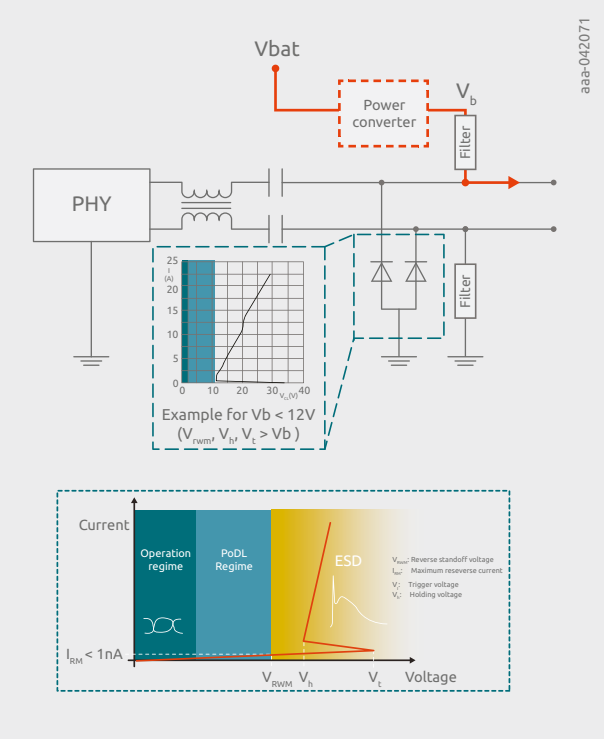

Figure 51 | Placement and properties of the ESD device on the connector side. The ESD device should withstand the power put on the data lines, which means the voltage ratings (Vrmw, Vh, Vt) should be higher compared to Vb as shown in the IV curve on the right.

The advantage of this position is that all components of the circuitry including the filters are protected by the ESD device and the ESD pulse is clamped to GND directly at the connector. The disadvantage is the higher voltage rating of the ESD device. If no CMC or other inductors or resistors are placed between the PHY and the ESD device then the IV-characteristics need to be matched to the internal ESD structure of the PHY. Especially for high-speed PHYs this is a critical point because most show a very low voltage rating of the internal ESD structure in the range of a few volts only. In this case the designer can decide whether to add some series elements such as inductors or resistors between the external ESD device and the PHY, or can place the ESD device on the PHY side behind the DC caps, as shown in Figure 52. Here, the DC caps block any DC power from the PHY and from the ESD device, which allows the use of an ESD device with a much lower voltage rating of a few volts only. In most cases, matching to the internal ESD structure of the PHY can be done very easily which results in a robust ESD design of the interface. However, it should be mentioned that all components which are on the connector side will be partially exposed to the ESD pulse and their selection should consider this fact.

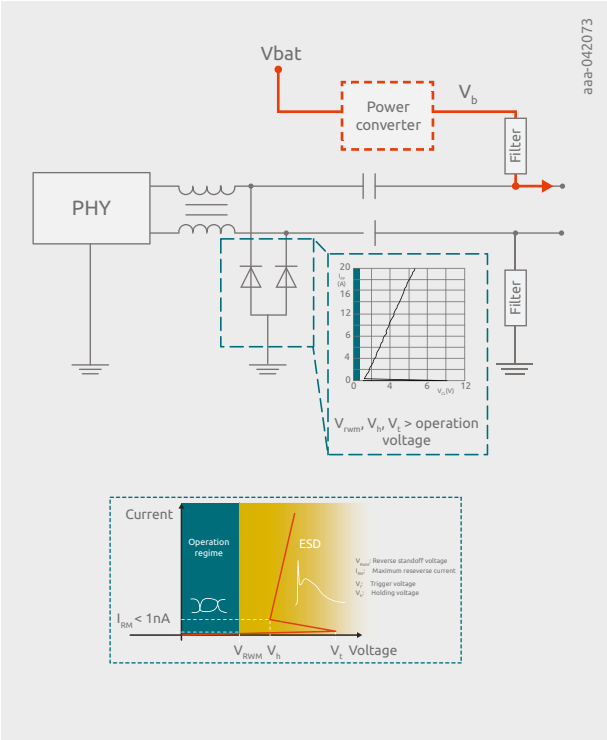

Figure 52 | Placement and properties of the ESD device on the PHY side. The ESD device does not need to withstand the power put on the data lines because of the DC caps, which means the voltage ratings (V_{rmw}, V_h, V_t) should be higher compared to the operation voltage (typically in the range of a few ~V for Ethernet and SerDes interfaces) as shown in the IV curve on the right

7.5.3 Automotive Ethernet

With the introduction of zonal architecture in modern cars, new interfaces were required to support the increased data processing. Automotive Ethernet emerged in the early 2010s with a speed of 100Mbit/s. To establish a standard, the OPEN Alliance SIG [10] was formed. The most challenging topics were electromagnetic compatibility (EMC) and the limitation to one single twisted pair only (the '1' in the prefix indicates one differential pair). In 2015 and 2016 the specifications were finalized for 100BASE-T1 and 1000BASE-T1. Currently, the specifications for 10BASE-T1s are close to finalization and MGBase-T1, which is a combination of three data rates (2.5 Gbit/s, 5 Gbit/s, and 10 Gbit/s), is in preparation.

Generally, unshielded twisted-pair (UTP) and shielded twisted-pair (STP) are allowed. However, for cost reasons and a high re-use potential from CAN applications, UTP is preferred. At data rates of 100 Mbit/s and above, all connections are point-to-point, and a central switch is required to create larger networks. The low-cost 10BASE-T1S however, allows several nodes to be connected to a single UTP cable. The physical layer is very close and sometimes compatible

with CAN (FD/XL). The work in the OPEN Alliance is coordinated with other groups like NAV Alliance, ASA and serves as preparation and augmentation for standards published via IEEE, SAE, and other standardization consortia. As with every automotive networking technology, the ESD requirements for automotive Ethernet are rather high. Usually, 15 kV contact discharge (IEC61000-4-2) on a module basis is the standard requirement, but some car OEMs may require 30 kV air discharge. In most test procedures demanded by car manufacturers, ESD is tested on the unpowered module with direct discharge on the communication pins and on the powered module with a connected cable. After the unpowered test, the module is connected to a reference system and checked for normal operation. Effects that may cause a failure in the unpowered test are destruction of or damage to the PHY and degradation of passive components in the signal path deteriorating signal integrity. In the powered test, there is the possibility of a non-destructive event in the PHY causing malfunction and errors in communication. This failure is usually called soft failure. A suitable ESD protection concept for an automotive Ethernet interface should prevent the PHY and passive components from destruction, degradation, or malfunction as the result of an ESD event, without impacting the system performance in any negative way.

Currently, four automotive Ethernet standards are finalized or close to finalization: 10Base-T1S, 100Base-T1, 1000Base-T1, and MGBase-T1. 25GBase-T1 is in the preparation.

Table 36: Overview of automotive Ethernet standards (UTP = unshielded twisted pair, STP = shielded twisted pair, SPP = shielded parallel pair)

	10Base-T1S 802.3cg	100Base-T1 802.3bw	1000Base-T1 802.3bp	MGBase-T1 802.3ch	25Gbase-T1 802.3cy
Data rate	10 Mbps	100 Mbps	1000 Mbps	2.5/5/10 Gbps	25 Gbps
Symbol rate	12.5 MHz	66 MHz	750 MHz	1.4/2.8/5.6 GHz	7 GHz
Line coding	4B/5B, PME	PAM3	PAM3	PAM4	PAM4
Distance	15/25 m	15 m	30 m	15 m	11 m
#Lanes	1	1	1	1	1
Cable transmission	UTP	UTP	UTP (STP)	STP/SPP	STP/SPP

In most cases the Ethernet network is build up in a point-to-point topology. This is valid especially from 100Base-T1 upwards. However, 10Base-T1s is mean to be easy and cost-reduced interface which should re-use most of the CAN and Flexray infrastructure for a bus topology. It is important to mention that up to 1000Base-T1 UTP are proposed in the standards. Those unshielded cables are just a single twisted pair – known from CAN interfaces – are exposed to a rough electromagnetic environment in the car since they are usually bundled in with other cables which introduces a risk of electromagnetic interference (EMI). Several investigations were done in from FTZ Zwickau, Germany to quantify this risk by performing bulk current injection (BCI) tests [12]. In this test, a 10Base-T1S UTP network consisting of 8 nodes was exposed to BCI Class IV disturbance up to 1000 MHz. A voltage probe was placed close to the CMC at the nodes to quantify the maximum voltage being induced in the unshielded cables. The results are somewhat surprising since at some frequencies the V_{RMS} can go up to 70 V, which also means that the peak voltage can go up to 100 V. This is interesting for a number of reasons, and is particularly relevant to ESD. Typical ESD protection devices usually trigger and activate far below 100 V. Once triggered during the communication, the data transmission will be disturbed, which is not wanted. The OPEN Alliance decided to specify the trigger voltage for external ESD protection devices as > 100 V for UTP cables. This is a special requirement in the industry and brings additional challenges for the interface as well as for the ESD protection device itself.

ESD protection for 10Base-T1s, 100Base-T1 and 1000Base-T1

As mentioned above, the main topology of 10Base-T1s, 100Base-T1 and 1000Base-T1 is very similar: UTP cables, standard connectors and the schematic are very alike (see Figure 50). Some differences can be observed in the properties of CMC, the values of the resistors in the common mode termination (CMT), and the transceiver itself [10]. This leads to mainly the same requirements on ESD and on ESD protection device with trigger voltage of > 100 V, as can be seen from the TLP plot in Figure 50. As mentioned above, this is mainly due to the UTP cables and a possible risk of noise coupling into the interface.

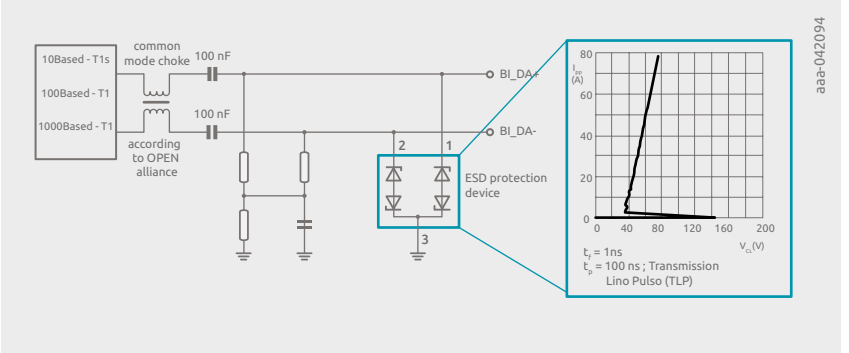

Figure 53 | Schematic for 10Base-T1s, 100Base-T1 and 1000Base-T1. Main structure of the interface is the same. Some differences can be found in the values of the transceiver, resistors, and CMC.

At this point it is important to mention that OPEN Alliance defines the Ethernet network in great detail. For the first time there are dedicated specifications for electronic components such as CMC and ESD protection devices. There are some general requirements defined for the ESD device shown in Figure 51.

Table 37: Fundamental requirements for ESD protection devices for 10Base-T1s, 100Base-T1, and 1000Base-T1 [11].

Parameter	Target Value
Working direction	bi-directional
Operation voltage (VDCmax)	≥ 24 V
ESD trigger voltage	≥ 100 V
ESD robustness against damage	+/– 15 kV contact discharge for unpowered device using discharge module according to ISO 10605 (discharge storage capacitor C = 150 pF and discharge resistor R = 330 Ω)
Minimum number of discharges	> 1000
TLP characteristic according to [IEC1]	I/V characteristics

Besides the high trigger voltage of >100 V mentioned above, there are some additional requirements such as minimum 15 kV contact discharge for 1000 discharges without destruction. In addition, there are several specific tests defined for the ESD protection device.

- Mixed mode S-parameter:
  To evaluate transmission, symmetry, and mode conversion
- Damage from ESD:
  To verify degradation in S-parameters after ESD (8kV)
- ESD discharge current:
  Quantification of the current that would flow into the PHY during ESD
- Unwanted clamping:
  Evaluate impact of ESD device on RF immunity testing
- Parasitic capacitance:
  To evaluate the parasitic capacitance of the ESD device

Table 38: Overview of additional tests for the ESD device based on the OPEN specifications [11] and requirements on the ESD protection device.

Test	10Base-T1S	100Base-T1	1000Base-T1
Mixed Mode S-parameters	x	x	x
Damage from ESD	x	x	x
ESD discharge current	x	x	x
Unwanted clamping	x	x	x
Parasitic capacitance	x		
Requirements on ESD Device			
V_{ESD}	> 15 kV	> 15 kV	> 15 kV
V_{RWM}	> 24 V	> 24 V	> 24 V
V_h	> 24 V	> 24 V	> 24 V
V_t	> 100 V	> 100 V	> 100 V
C_D	< 2 pF (< 0.5)	< 3 pF	< 2 pF

Most of the tests must be carried out for the ESD devices for all three automotive standards. However, only the parasitic capacitance test is required for 10Base-T1S, due to the large number of nodes (up to 50) and, hence, strong limitations of total capacitive load. As we also see from Table 36 the requirements on the ESD protection device are very similar. As already mentioned above, this is mainly due to the circuitry and UTP cables. The main difference is the device capacitance due to the large number of nodes for 10Base-T1S.

It should be noted that, especially for 1000Base-T1, in some cases shielded cables are used. As discussed in [12] such shielded cables (e.g. shielded twisted pair, STP) might have significant benefits especially in their EMC performance, since the radiated emission can be dramatically reduced. Shielded cables typically have a shielding efficiency of > 40 dB or even > 60 dB, which significantly reduces the electromagnetic interference compared to UTP, as described in detail in the next section. This implies that the high trigger voltage (Vt) requirements > 100 V in Table 36 are not valid. In this case, much lower trigger is a better choice.

ESD protection for MGBase-T1

Increasing demand for connectivity and data processing requires higher data rates for automotive Ethernet. OPEN Alliance is creating a standard for this so called multigigabit Ethernet, MGBase-T1, which consists of three different speed grades: 2.5 Gbps, 5 Gbps and 10 Gbps (see Table 35). This is in general a point-to-point communication protocol based on single shielded differential pair. The standard and the circuitry are currently under discussion and not finalized, but will probably be different to 1000Base-T1 due to the shielded transmission. Some components, such as CMC and the CMT, are not mandatory and especially for the speed grade 5 and 10 Gbps will probably not be used. For ESD protection, there are two possible options, as shown in Figure 52.

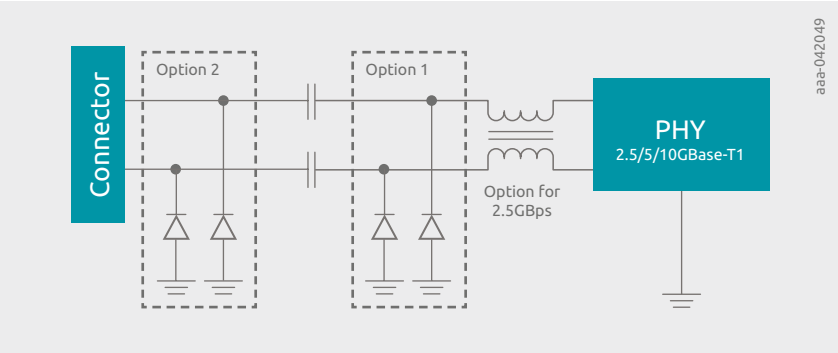

Figure 54 | Circuitry of the MGBT1. The CMC will be mostly not required and probably limited to 2.5 Gbps speed grade. Two ESD options are possible option 1 on the PHY side and option 2 on the connector side.

There are pros and cons for both options:

Option 1:
The ESD device is not exposed to short to battery and hence an ESD device with much lower voltage rating can be chosen. This is a significant benefit since the lower the clamping voltage the less ESD stress for the PHY. In addition, lower voltage rating can be key when no CMC is used because in this case the clamping voltage ESD device should be lower compared to the internal ESD structure of the PHY.

Option 2:
The ESD device is exposed to short to battery and hence the voltage rating will be higher than the battery voltage. In a combination with a CMC with an inductance in the range of ~100uH this is a very robust solution against ESD. If a CMC is not present, then it should be confirmed that the clamping voltage on internal ESD structure of the PHY is not clamping lower than the external ESD device to ensure proper ESD robustness.

Based on experience so far with MGBase-T1 PHYs and other high-speed PHYs, Option 2 can probably only work with a CMC in place. This is a consequence of the low-voltage internal ESD structure PHYs and a general trend which can be observed in high-speed ICs for infotainment interfaces. In some cases, the short to battery test is not required. Which means the ESD device should be always placed at the connectors side (Option 2).

Automotive Ethernet >10Gbps

There are two strings of high-speed ethernet beyond 10 Gbps. One is the working group P802.3cz which looks at the standard on the implementation of the optical link into the automotive environment with up to 50 Gbps over a 40 m fibre-optics [13]. The other is 802.3cy, with the classical approach of wired point-to-point communication up to 25 Gbps over 11 m cables [14].

From the standpoint of ESD, there is a focus on wired interfaces 802.3cy. Since there is focus yet on ESD protection devices. Based on experience from latest consumer interfaces in similar data rate range, e.g. USB 3.x and USB 4.x, and from 802.3ch the ESD protection device need to cover very low voltage ratings < 5 V and lowest clamping voltages. In addition, there will be very challenging SI requirements in a bandwidth up to 9 GHz which only can be handed with modern Si technology, very low Cd ~0.1 pF or below and a very compact package such as FCLGA or SOD962 with very small parasitics to comply SI requirements.

7.6 Serializer/deserializer interfaces

Serializer/deserializer (SerDes) is an umbrella term describing the use of serial interfaces to transmit data from a parallel data stream. These interfaces are high bandwidth, point-to-point by design, and latency is usually not critical. They are usually unidirectional, or bidirectional where the bandwidth in one direction is significantly higher (> 10 Gbps) than in the other (< 5 Gbps). The physical implementation of the serial data stream can be differential, using low-voltage differential signaling (LVDS), or single ended using a coaxial cable. Optical links are also possible but are not discussed here.

SerDes interfaces with a single-ended physical layer are sometimes used to transmit power to the ECU as well as the data stream. For coaxial single-ended links, this technique is called power over coax (PoC), in a similar way to power over data line (PoDl) and power over Ethernet (PoE).

SerDes interfaces are mainly used to transmit video data. The most common applications are in infotainment to connect displays, in parking cameras, and in cameras used for ADAS applications. With an increasing demand for ADAS applications due to the growth in popularity of autonomous driving, SerDes interfaces are becoming key interfaces in the automotive sector.

For cameras, PoC functionality is particularly beneficial. In a modern zonal architecture, SerDes interfaces are the exceptional point-to-point connections that are required to make high-resolution sensor data available.

Proprietary SerDes solutions are common in the automotive industry. Although the non-profit Automotive SerDes Alliance (https://auto-serdes.org/) is working to standardize SerDes interfaces, no specification is currently available.

Here, we provide an overview of three different proprietary implementations.

7.6.1 Automotive Pixel Link

Automotive Pixel Link (APIX) was designed by Inova Semiconductors and licensed in 2008 by Fujitsu. It can be used to transmit digital video signals over a distance of up to 15 m. The third-generation generation of the technology, APIX3, has been available since 2016. Since APIX2 the standard has supported bi-directional protocols as well as unidirectional video transmission. APIX2 supports a 720 p video signal and additional communication over SPI, I²C, or Ethernet using the same interface. APIX3 supports data rates up to 12 Gbit/s with the STP (shielded twisted pair) and up to 6 Gbps with the QTP (quad twisted pair). Depending on the mode of operation, one or two STPs or QTPs are required. Furthermore, APIX allows data lines to be used as a power supply for the modules. With power-over-APIX (PoA),

the differential data lines can also be used to provide power to the serializer side. When PoA is used, the protection must be selected accordingly. The protection is located either behind the decoupling capacitor, so the same protection that would be used without PoA is used, or at the connector. In that case, the protection is not allowed to clamp below the supplied DC voltage, to prevent latch-up.

7.6.2 Flat Panel Display Link

Flat Panel Display Link (FPD-Link) was originally designed for displays but is also often used to connect cameras to ADAS computing units. It was created in 1996 by National Semiconductor for use in laptops and TVs. Today, FPD-Link is owned by Texas Instruments and popular for automotive ADAS applications. The second-generation FPD-Link introduced communication via a single LVDS channel on an STP cable up to 10 m, achieving data rates up to 1.8 Gbit/s. FPD-Link III allows for data rates up to 13.3 Gbit/s and bidirectional communication on a single link. Additionally, FPD-Link III allows the use of coaxial cables and PoC. FPD-Link serializes parallel TTL, LVCMOS, LVDS signals, or MIPI.109 108.

7.6.3 Gigabit Multimedia Serial Link

Gigabit Multimedia Serial Link (GMSL) is a proprietary SerDes interface introduced by Maxim Integrated that is mainly used for camera and display applications. The second generation introduced in 2017 features LVDS over STP and single-ended coaxial operation with cables up to 15 m. The maximum data rate goes up to 12 Gbps and interfaces with LVCMOS, CMOS, LVDS, MIPI and HDMI. Communication is unidirectional with a bidirectional control channel. GMSL supports PoC with 5 V and 12 V.

7.6.4 The Automotive SerDes Alliance

APIX, GMSL, FPDLink are all proprietary interfaces. The Automoative SerDes Alliance (ASA) is working in a similar way to the OPEN Alliance to standardize an asymmetric SerDes interface for automotive applications. The standardization includes the physical layer, data link and transport layer at up to 15 m over coaxial and 10 m over shielded differential pair (SDP) transmission. There are five speed grades with data rates up to 16 Gbps over PAM4 and a downlink of over 100 Mbps (Alliance, 2024).

Table 39: Overview of speed grades within ASA (Alliance, 2024)

Speed Grade	Donwspream/ Upstream (Gbps)	Modulation	Bandwidth (GHz)
1	2/2	PAM2	1.4
2	4/4	PAM2	2.8
3	8/4	PAM2	5.6
4	12/4	PAM4	4.2
5	16/4	PAM4	5.6

As can be seen in Table 39, there are five speed grades with an upstream of up to 16 Gbps. The physical bandwidth is also dependent on the speed grades and reaches up to 5.6 GHz. This influences the choice of suitable ESD protection device, which needs to have a very low device capacitance of less than 0.5 pF. Packages also need to be selected carefully. A compact solution such as DFN1006, DFN1006LD as a three-pin or as a two-pin option (FCLGA) and SOD962 (DSN) should be used.

7.6.5 MIPI A-PHY

The MIPI Alliance supports several standards for transmission of video data (see Section 9.3). With a similar goal to the ASA (Alliance, 2024), the MIPI Alliance is preparing a non-proprietary SerDes standards called A-PHY [15]. The first version released in 2020 features up to 16 Gbps on cables up to 15 m in length. A-PHY supports differential communication on STP cables and single-ended communication on coaxial cables, with power over coax. MIPI A-PHY is meant to directly interface with the existing MIPI Physical Layer Standards C-PHY and D-PHY, and operate in the CSI-2 protocol.

The MIPI Alliance and ASA are liaising on their standard-development work.

7.6.6 ESD device requirements for SerDes interfaces

The requirements for external ESD protection are similar for all SerDes interfaces and state-of-the art protection technology is required. Protection devices used in the computing industry to protect high-speed data lines with extremely low capacitance are suitable for this task. Multiline protection devices designed for USB can often be reused to protect LVDS interfaces. A low parasitic capacitance is essential to maintain signal integrity. As the parasitic capacitance is lower than 1 pF, the matching of line capacitances for differential signaling is not critical and single-line protection devices are applicable. Single-ended coaxial interfaces are

protected using single-line protection devices Since all SerDes interfaces operate in a high Gbps range, there is a strong requirement on getting the signal transmitted over 10 or 15 m cables. Interfaces usually come with shielded cables, coaxial or STP. Also the connectors (Fakra, HSD, HMTD, for example) are shielded and very well defined for signal Integrity purposes. In this context, there is no need to have an ESD protection device with a trigger greater than 100 V, as we know from 100/1000Base-T1. Similarly, as for USB or HDMI interfaces, low-voltage ESD devices with very low clamping are required here. This is illustrated by the IV-characteristics shown in Figure 55. Here, we see some PHY with a very low breakdown voltage of ~ 2–3 V and some at ~ 20 V. As, in most cases, no series elements such as ferrite beads, CMC, resistors etc are placed in between the external ESD device and the PHY, only an ESD device with very low clamping characteristics should be used here. Otherwise, the interface cannot be protected adequately.

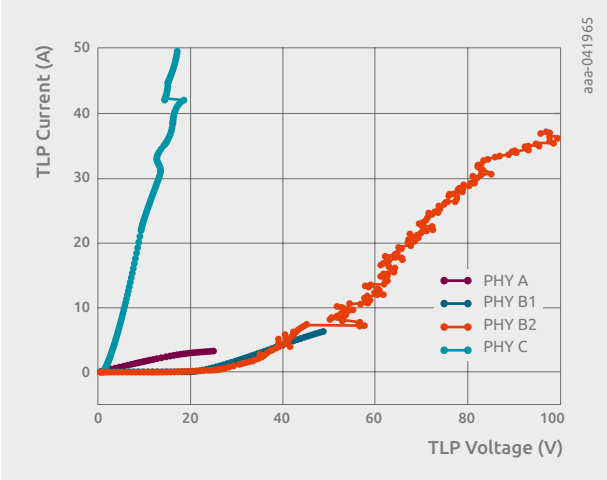

Figure 55 | IV performance of different automotive SerDes interfaces showing the ESD characteristics of the on-chip protection. Note the broad range of breakdown voltages.

Both power-over-data-line and power-over-coax (PoC) are common and widely used, especially with GMSL and FPD-Link cameras in surround view and ADAS applications. Although there is a general trend to simplify wiring and reduce the amount of copper used, ADAS applications in particular show a broader use of this technique due to the high number of sensors they use. The general principle is shown in Figure 56. Power is supplied to the serializer side from the deserializer side using appropriate filters, in this case simple inductors L1 and L2 and decoupling capacitors (decaps). The EMC requirements of the power source and regulator are very high to maintain signal integrity and avoid spoiling the data signal. There are different options for positioning external ESD protection devices. The goal is here to protect the high-speed interface. The power regulator input and

power source output can be protected by ordinary TVS devices behind the filter. For the high-speed interface the protection can be placed at the connector (ESD_1), behind the decap (ESD_2), or both.

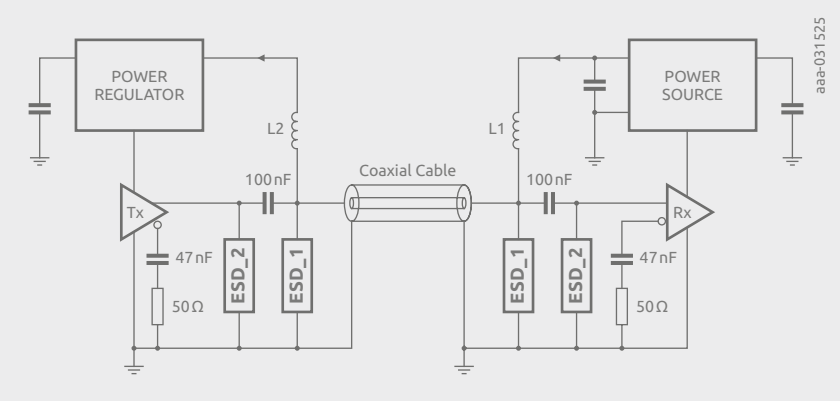

Figure 56 | Generic interface for SerDes with PoC and two positions for ESD protections

In general, placing at the connector should always be preferred because it provides the best protection performance. However, the protection device must be selected so that it can operate with the DC bias and since no series element (ferrite bead, resistor or CMC, for example) is used it should match the internal protection of the Tx/Rx. For protections behind the decaps, only the data signal levels need to be considered. In general, snap-back devices are also applicable at the connector if there is no risk of latch-up. As it is very difficult to assess this situation on a purely theoretical level, in-application test are inevitable to ensure that the application is protected and there is no risk of latch-up. The challenge is that in the application, a snap-back seen in TLP and a risk of latch-up do not necessarily correlate. There are devices that show a small snap-back in TLP but do not latch-up when tested in the lab. On the other hand, there are devices that show a snap back in TLP but can latch-up at voltages lower than seen from TLP when stressed with surge pulses. This different behavior depends on the technology and details of how it is implemented, and cannot be expressed in general terms in the datasheet as the results may vary with the applied DC source and the applied pulse. When testing for a latch-up, it is important to use the same power supply characteristics, in terms of load line, regulation scheme and speed. In many cases, the sources used in the application are not able to provide enough current within the short time of a transient event to actually cause a latch-up. Devices with a relatively shallow snap-back are usually very robust against latch-up. On the other hand, some technologies show several snap-backs which may not be seen from the datasheet because they are only triggered with very long pulse durations. A latch-up test with

a realistic power supply and the relevant transients provides clarity and confidence.

Considering the fact that the ESD device for SerDes interfaces should provide robust performance in any position, including according to the special requirements of PoDL/PoC and short to battery, the position ESD_2 close to the PHY shown in Figure 57 seems to be the most promising.

Figure 57 | IV characteristics of two different PHYs and the ESD protection device for both ESD positions. A low-voltage ESD device (right) can protect both PHYs, a higher-voltage ESD device (left) can protect only one PHY.

7.7 Antenna interfaces

RF antennas are the cornerstone of wireless communication. They transmit and receive data between devices and network base stations by converting electromagnetic waves into electrical current and vice versa.

Regardless of whether an antenna is receiving or transmitting, the accuracy of the signal is key to ensuring good communication. This means that the design of antennas, as well as the receiving and transmitting circuits must adhere to stringent signal integrity standards. In particular, components that are added to an antenna system should not interfere with the signal, to maintain optimum performance.

The following sections outline the properties and requirements of different kinds of antennas and antenna interfaces. They also introduce methods that can be used to quantify the impact of ESD protection devices on antenna systems and show how to apply them in selected use cases.

7.7.1 Commonly used RF frequencies

Wireless communication frequencies today span the frequency range between roughly 500 MHz and 50 GHz. Popular frequency bands are 800 MHz, 1 GHz and 2 GHz. Figure 58 illustrates the frequency ranges for the most widely used RF communication standards.

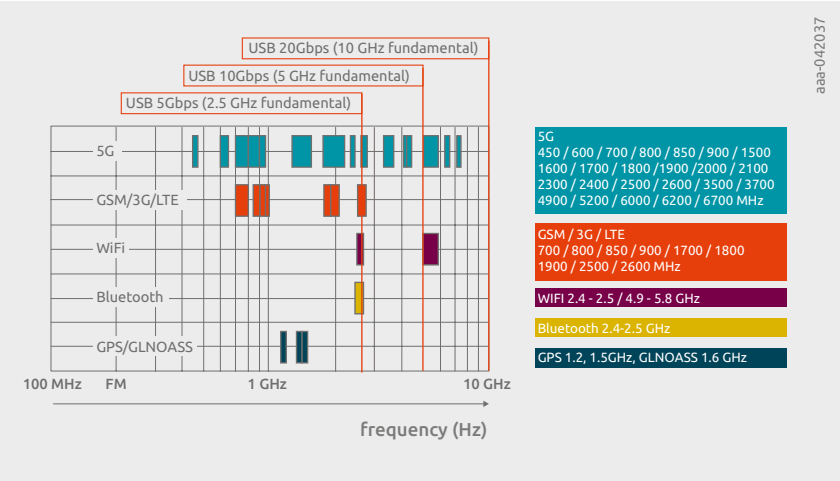

Figure 58 | Wireless communication frequencies

One important characteristic of ESD pulses is the very fast rise time of the 1st peak, which is specified to last less than 1 ns. This is one of the reasons why the output frequency spectrum of ESD generators also covers the frequency range around 1 GHz. This unfortunate coincidence means that RF inputs of cellular communication chipsets can be very ESD sensitive, due to the fact that their input frequency range overlaps with the output frequency range of ESD generators [16].

7.7.2 Antenna connectors

Antenna connectors are used to connect RF circuits to an external antenna for better signal transmission and reception. In today's consumer electronics applications, this is often the case for Wi-Fi signals, as shown in Figure 59.

Figure 59 | External antenna connector

Although many wireless communication devices don't have externally visible antennas, they often use antenna connectors for various purposes. For example, connectors like U.FL are used to distribute multiple antennas within the case of Wi-Fi access points and routers. In smartphones, the same technique is used to connect antennas in the lower part of the handset to the RF receivers and transmitters on the mainboard in the upper part of the device. If the distance to the antenna is smaller, small spring-loaded contacts can be used to attach to it. Examples of this approach are shown in Figures 60 and 61.

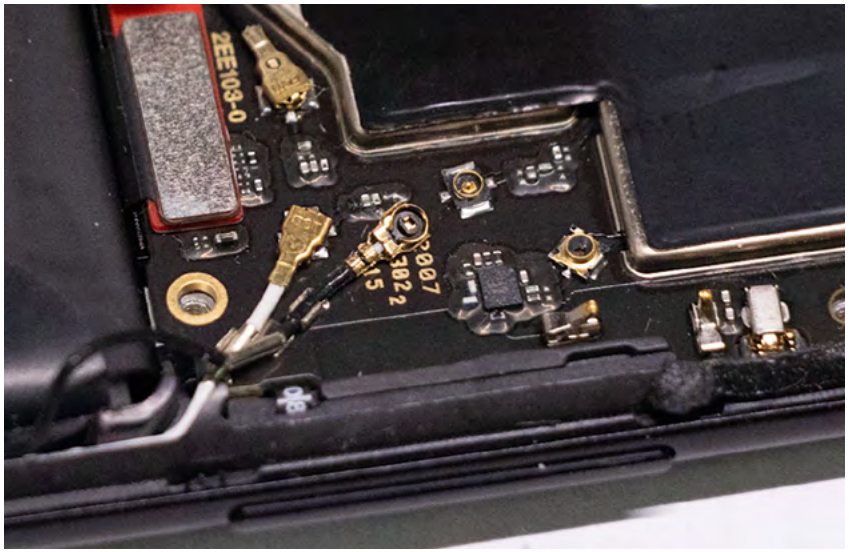

Figure 60 | Internal antenna contacts

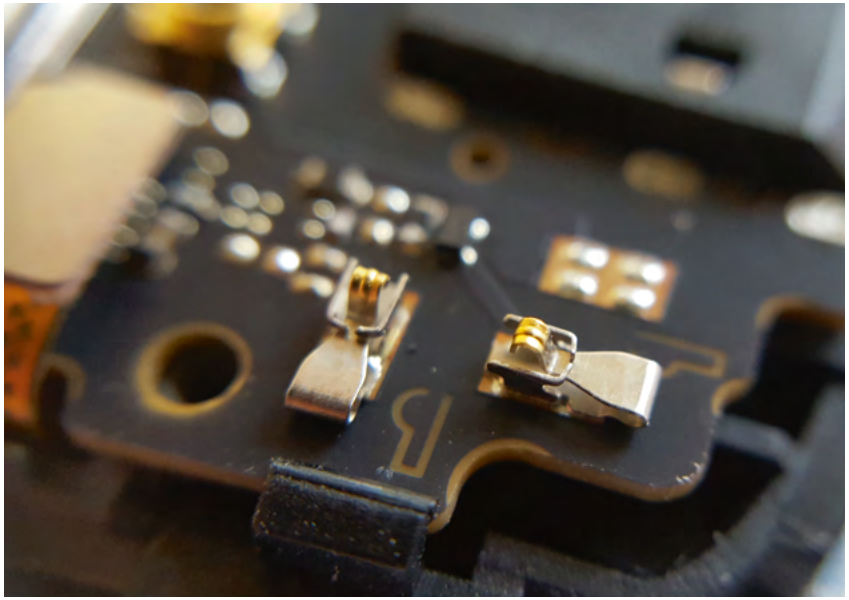

Figure 61 | Internal antenna terminal

Another reason for placing antenna connectors in RF communication devices is to add a port for testing and tuning during production. An example of this type of connector is shown in Figure 62.

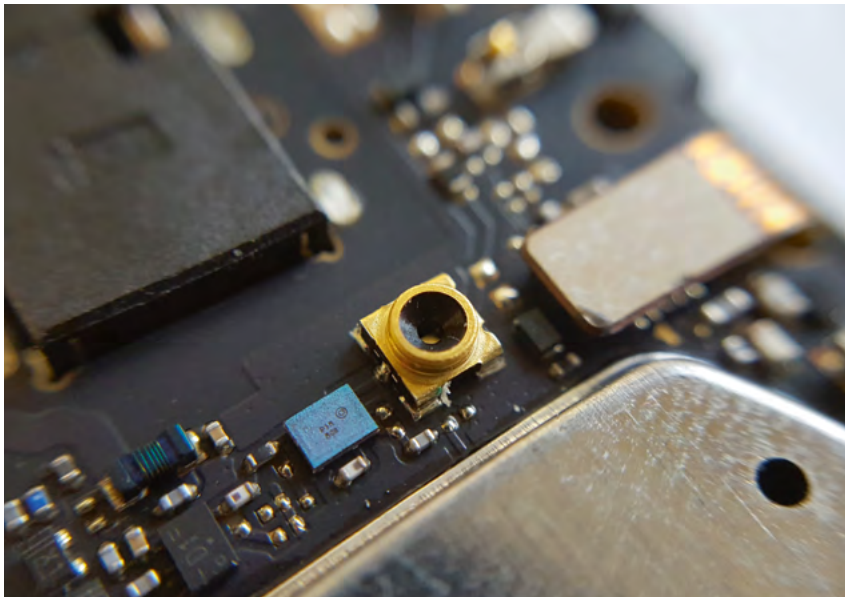

Figure 62 | Internal antenna interface

No matter what purpose an antenna connector serves, it always provides ESD discharges with a potential point of entry into the system. While externally accessible connectors are more prone to receiving ESD strikes, internal connectors can cause damage to sensitive RF circuits if they receive an ESD strike during device assembly or from the outside via gaps in the casing. In this situation, a common rule of a thumb is that ESD discharges can cross a distance of roughly 1 cm per kV.

Choosing the right external ESD protection can help increase a system's ESD robustness. The following sections outline what criteria need to be considered when using an ESD protection device at an antenna port.

7.7.3 Requirements for RF antenna ESD protection

What properties are required for a protection device that is applied at an antenna terminal?

It is inevitable that a protection device has a capacitance. To minimize its impact, the capacitance should not limit the RF signal's high frequencies and should therefore be as small as possible. Besides the size of the capacitance, it should also have high linearity to avoid distortion. This means the C_d over voltage curve should be as flat as possible in the target frequency band of the application.

Additionally, a protection device should not limit the signal amplitude with its clamping characteristics. Thus, the breakdown voltage and subsequently the maximum reverse working voltage V_{RWM} should be larger than the maximum signal amplitude at the antenna terminal.

Ultimately, an ESD protection device that is added to an RF signal line should not cause any change to the transmitted signal – i.e. it should not cause any distortion. The best way to assess this is to measure its harmonic distortion.

Any non-linearity will have an impact on the transmitted signal wave. While some effects are obvious, others like capacitance, can also influence the frequency of a transmitted signal. The following sections look at some of these effects in more detail.

Capacitance

In the first approximation, the ESD protection device that is placed on an RF antenna line, can be regarded as a capacitor whose capacitance can affect the transmitted signal in several ways. First, it will act as a low-pass filter, limiting the maximum frequency. The capacitance alone will not generate harmonics, but may alter the transmission based on the characteristics in the following formula

$$H(s) = \frac{1}{s \cdot RC + 1}$$

Another effect comes into play when the capacitance has a non-linear characteristic, as is the case for ESD protection devices. Considering that the capacitance value changes over voltage, different amplitudes of the signal will see different attenuation as shown in the following figure.

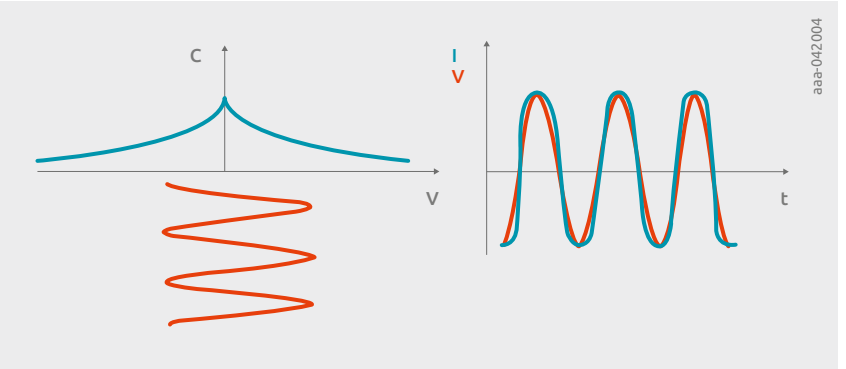

Figure 63 | Distortion caused by voltage dependent capacitance

An example of the voltage dependence of an ESD protection device is shown in Figure 64. Clearly, less dependence, or in other words a flatter C(V) characteristic, is a better option for use with RF antennas.

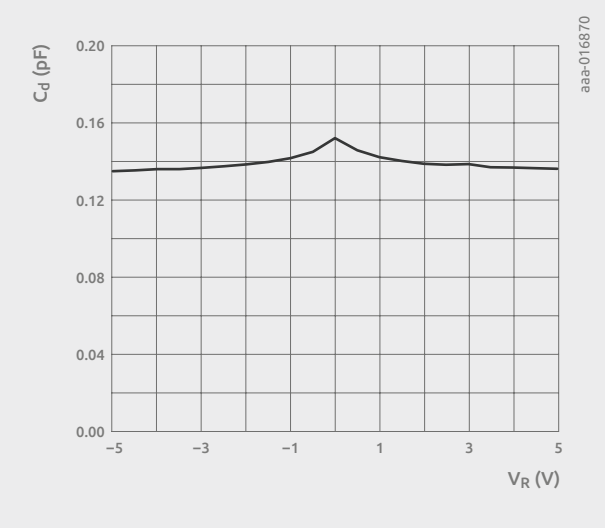

Figure 64 | Voltage dependent capacitance of an ESD protection device

A second factor that influences the capacitance is the frequency. An example of this dependence for an ESD protection device is shown in Figure 65.

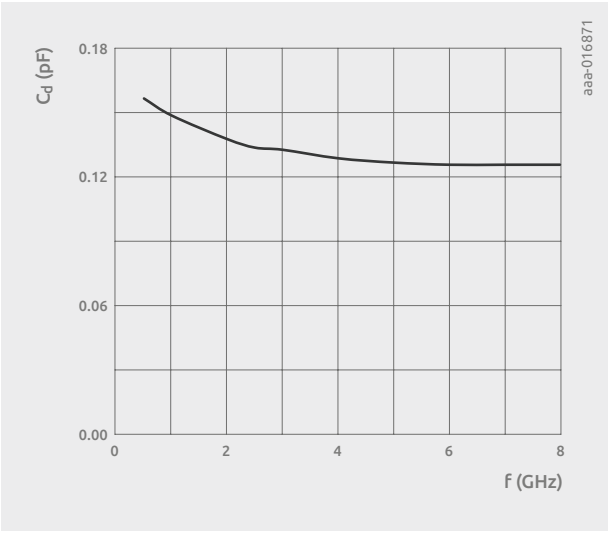

Figure 65 | Diode capacitance as a function of frequency

Insertion loss and return loss

Placing an ESD protection device on an antenna signal line will result in it interacting with the signal. It can be thought of as a two-port device as shown in Figure 66.

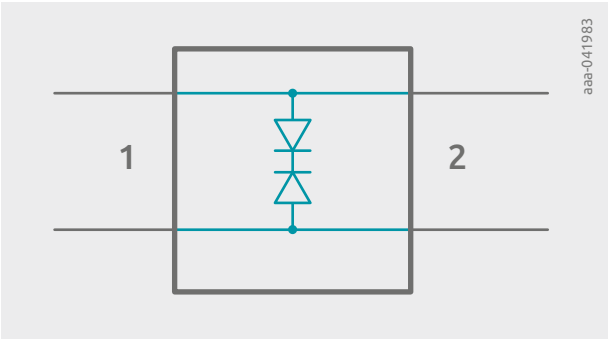

Figure 66 | ESD protection as a two-port device

When a signal is applied to port 1, the part of the signal that is lost when passing through the protection device to port 2 is the insertion loss. It is also known as attenuation and its size is proportional to the ratio of the power of the generator on port 1 to the power of the signal behind port 2. Knowing these powers, the insertion loss can be calculated using the formula below.

$$IL_{db} = 10\ log\ \frac{P_1}{P_2}$$

The insertion loss is measured in decibel and for the protection devices it is usually frequency dependent. Measuring the insertion loss for a certain frequency range yields a chart like the one shown in Figure 67.

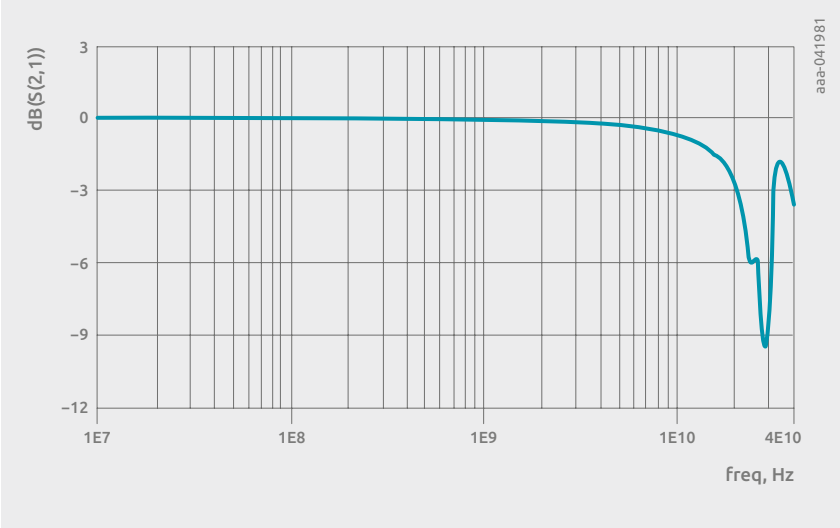

Figure 67 | Insertion loss graph

This shows clearly the typical low-pass filter characteristic of a protection device. Attenuation increases at higher frequencies, limiting their transmission. A key point in this context is the 3 dB bandwidth, which can be easily determined from the insertion loss chart. When selecting a device for antenna port protection, the insertion loss characteristic, especially the bandwidth, needs to be taken into account.

A second important parameter that describes the behavior of a protection device acting as a two-port device is the return loss. This is the part of the signal that does not get past the device (from port 1 to port 2) but is reflected at the entry port 1. Like the insertion loss, it is proportional to the input power (P_1) divided by the power of the reflected signal content (P_r). Its exact calculation is shown in the following formula:

$$RL_{db} = 10\ log\ \frac{P_1}{P_r}$$

Like the insertion loss, the return loss is measured in decibels (dB) and is frequency dependent. Its frequency characteristics for a typical protection device are shown in Figure 68.

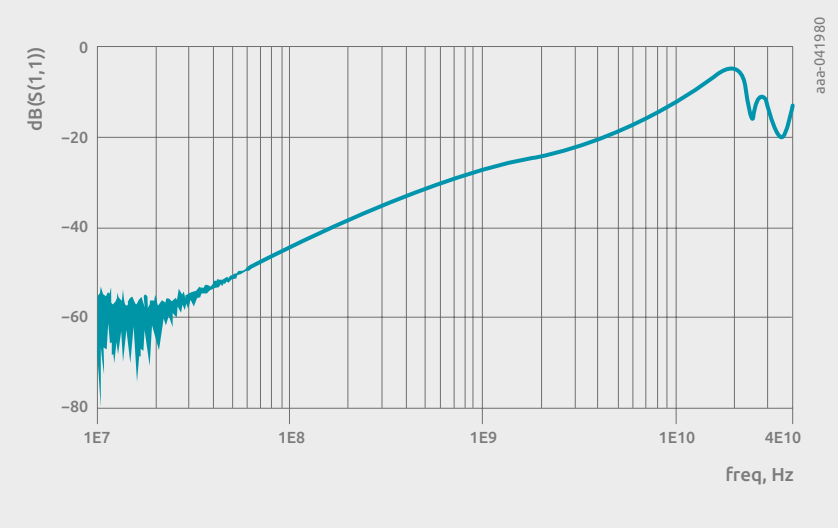

Figure 68 | Return loss

Section 6.1 of this book explains how insertion loss and return loss are measured and how they are represented in scattering parameters.

Clipping

As a non-linear device, an ESD protection component will start conducting once a certain voltage threshold is reached. If the amplitude of an RF signal is higher than the turn-on threshold voltage of a protection device, it may clip the signal and cause severe distortion.

A protection device therefore needs to be chosen that does not limit the RF signal amplitude. In particular, uni-directional devices with a forward voltage typically below 1V can limit the amplitude or cause clipping if the signal oscillates around 0V, as shown in Figure 69.

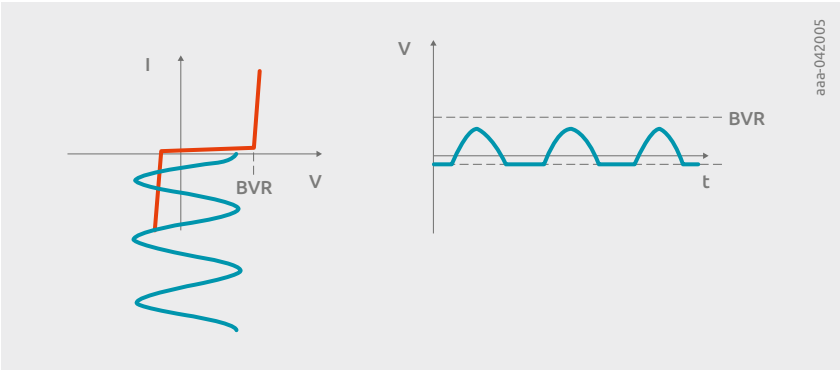

Figure 69 | Clipping of the negative signal content in a uni-directional device

The natural choice to prevent this behavior is to use a bi-directional protection device with a symmetric turn-on voltage for both negative and positive voltages. If the amplitude is too high, the signal may be clipped as shown in Figure 70.

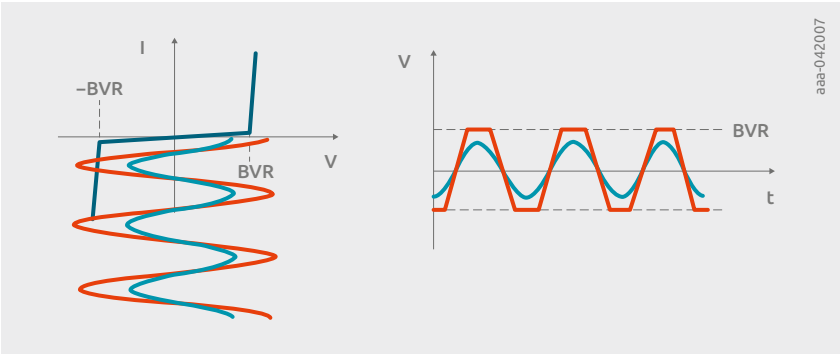

Figure 70 | Distortion caused by clipping in a bi-directional device

To avoid any clipping, a bi-directional protection device with high enough reverse working voltage (V_{RWM}) should be selected. (See Section 4.9 for more information about V_{RWM}.) Depending on the exact circuit and antenna design, the amplitude of a transmitted signal can reach voltages in excess of 10 V. It is not surprising that, for RF antenna protection devices with V_{RWM} in the range of 12 to 30 V are commonly used.

If a signal waveform is clipped it fundamentally changes the signal waveform, causing changes in the frequency content of the signal.

Harmonic distortion

For every signal transmission, the ultimate goal is to receive the signal exactly as it was transmitted. Deviation between the input and the output signals is regarded as distortion. Harmonic distortion refers to the generation of overtones, which are whole number multiples of the base frequency.

As shown in the following formula, summing the powers of all harmonic components and dividing by the power of the fundamental frequency yields the total harmonic distortion (THD).

$$THD = \frac{(P_2 + P_3 + P_4 + \ldots + P_n)}{P_1}$$

This ratio gives an indication of how large the content of harmonics in the signal is, compared to the fundamental signal. If there are no harmonics, THD will be zero any value higher than that indicates an increased amount of harmonics

Measuring harmonic distortion

Measuring harmonic distortion requires a carefully tuned test set-up with high-precision instruments. The set-up that is used by Nexperia to characterize our devices is shown in Figure 71.

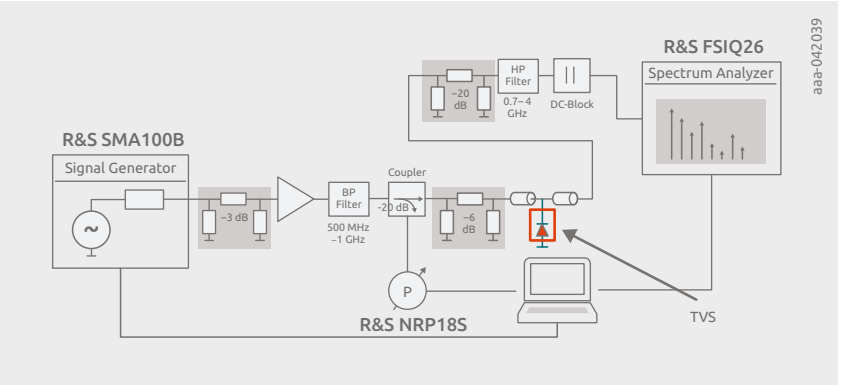

Figure 71 | Harmonic distortion measurement set-up

Measurement starts with a sine wave signal of the intended fundamental frequency being generated by the signal generator. The signal passes through a –3 db attenuator before it is amplified. After amplification, the signal is filtered by a band-pass filter that suits the intended fundamental frequency range. For the purpose of measuring the power of the input signal, a directional coupler feeds a –20 dB branch from the signal to a power sensor. The main signal path is then attenuated by –6 dB before it is applied to the DUT.

After passing the DUT, the signal is attenuated by –20 dB and filtered by a high-pass filter. As a final stage in the signal pass, a DC-block capacitor ensures that no DC content remains. The final instrument in this set-up is a spectrum analyzer.

All active components like the signal generator, the power meter and the spectrum analyzer are connected to a a central control PC to set the measurement parameters and read the results.

A measurement for a given frequency begins by setting the signal generator to this fundamental frequency and a defined output power. After the set-up has settled to this frequency, the transmitted power of the fundamental waveform is measured by the power meter and the spectrum analyzer. Performing the measurement multiple times for signals with increasing input power, and evaluating the output power behind the DUT for the fundamental frequency and multiples of it, yields the required harmonic distortion characteristics of a device as shown in Figure 72.

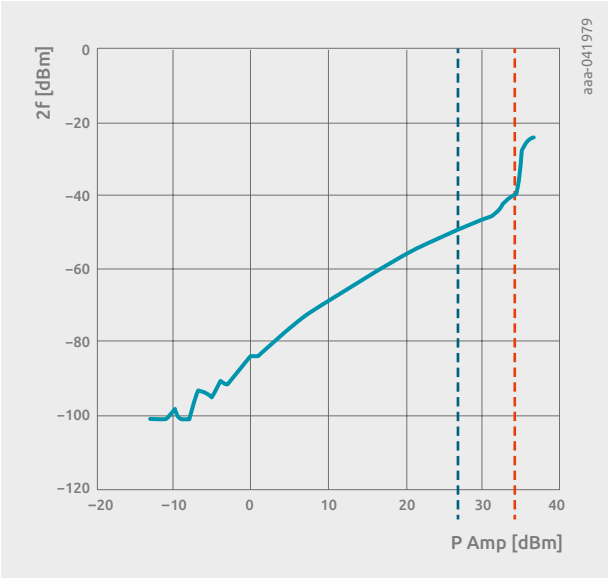

Figure 72 | harmonic distortion characteristics of an ESD protection device

The harmonic distortion plot for a given fundamental frequency shows the generated harmonics for a multiple of the fundamental frequency (in the example shown in Figure 72, this is twice the fundamental frequency). In the plot, the output power of the generated harmonics in dBm is plotted over the input power of the fundamental (also in dBm). For increasing input power, usually the harmonic output also grows. At an input power of 35 dBm, Figure 72 also shows a case where the device characteristic leads to an abrupt increase of generated harmonics. This could, for example, be due to clipping. A harmonic distortion limit in dBm that a given application imposes can easily be verified in such a plot by selecting the required value on the y-axis and checking whether or at which input power the measurement curve crosses the limit.

Measuring ESD protection devices is not in straightforward in all aspects. Depending on the internal structure of a device it may charge up during the measurement, which alters the result. While this process may take time, the result of the harmonic distortion measurement changes if a settling time is introduced, which allows the system to stabilize before taking the output readings. To illustrate this, Figure 73 shows the result of harmonic distortion measurements with varying settling time. In all characterization measurements of Nexperia parts, appropriate settling times are taken into account.

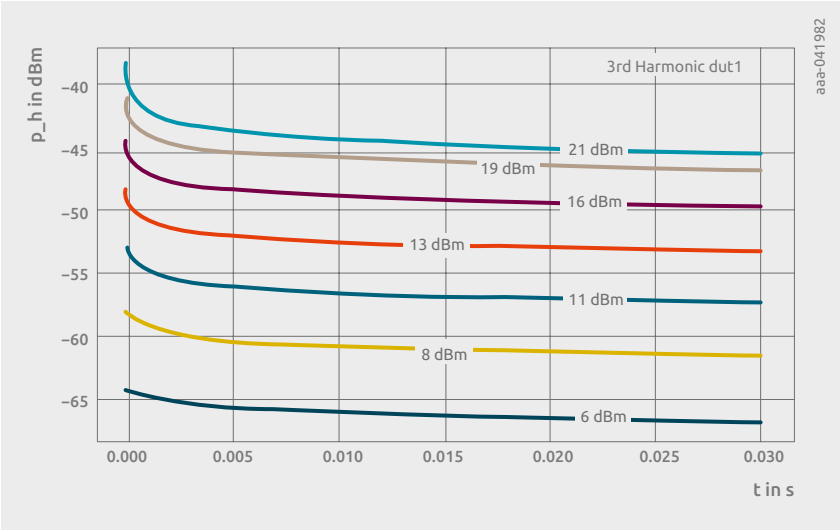

Figure 73 | harmonic distortion measurements with varying settling time

7.8 Supply line protection with TVS diodes

7.8.1 Introduction to supply line protection

Transient voltage suppressors (TVSs) protect interfaces other than data lines against overvoltages. When placed on a signal or supply line connected to a sensitive component (e.g. a highly integrated SoC), harmful overvoltages can be discharged through the protection device.

Sources of high-current surge pulses can be external or internal. External surge events can originate from, for example, the power grid, an external power supply or a discharge event from a charged cable. Internal surge events can originate from sources such as switching events or load changes.

Nexperia terminology denotes the difference between ESD protection products and TVS products. TVS protection devices (PTVS) can withstand significantly higher energy originating from high-current surge pulses and are meant to be placed on supply lines. In literature, and according to some protection device suppliers, both protection devices can be classified as TVSs.

7.8.2 Pulse standards

Depending on the source of the pulse it may have different pulse shapes (i.e. pulse length and rise/fall times) and energy. Common surge pulse standards are described in Chapter 5. It is worth noting that although standards like IEC 61000-4-5 are intended to describe the direct or indirect effect of lightning strikes on power lines, devices that are tested to this standard are not subject to these events. The test methods are used to characterize device robustness against other events that contain a similar amount of energy and have similar pulse shape.

7.8.3 TVS operation

As long as the voltage on the protected line stays below the breakdown voltage of the TVS diode, it does not react. Once the voltage on the line reaches the protection device's breakdown voltage, it will start conducting current to ground resulting in the voltage to be clamped to V_{CL}.

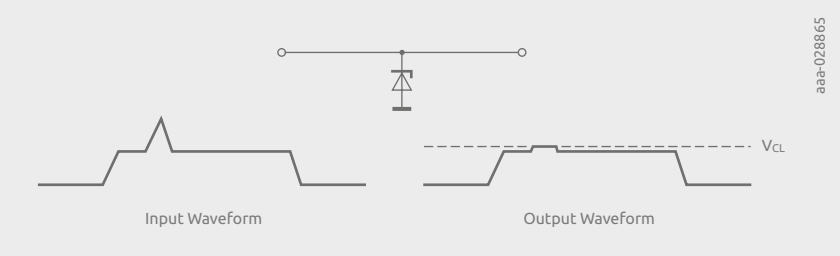

Figure 74 | Operation of a TVS diode on signal line

Based on the fundamental parameters of a TVS protection device with breakdown voltage V_{br} and dynamic resistance R_{dyn} (see Chapter 2), the clamping voltage for the peak current of a pulse can be calculated by

$$V_{CL} = V_{br} + I_{PP} \cdot R_{dyn}$$

7.8.4 Typical applications in a portable device

As surge events are commonly expected to enter a portable device using the power (charger) input, this is the most prominent place where TVS protection is applied. Figure 75 illustrates this. Optionally there may be a need to add secondary protection behind the charger switch or overvoltage protection (OVP) to protect the adjacent charger or power management components.

Due to increasing sensitivity of internal system blocks in a battery-operated device, additional TVS protection components may be required at the point of load. This helps to protect sensitive system blocks against harmful surge events that may occur on internal supply lines. Common examples are RF power amplifiers, which tend to be sensitive to overvoltages on the supply input. Placing a TVS protection with the appropriate breakdown voltage and low dynamic resistance on the supply lines of these ICs can successfully protect them against overvoltages.

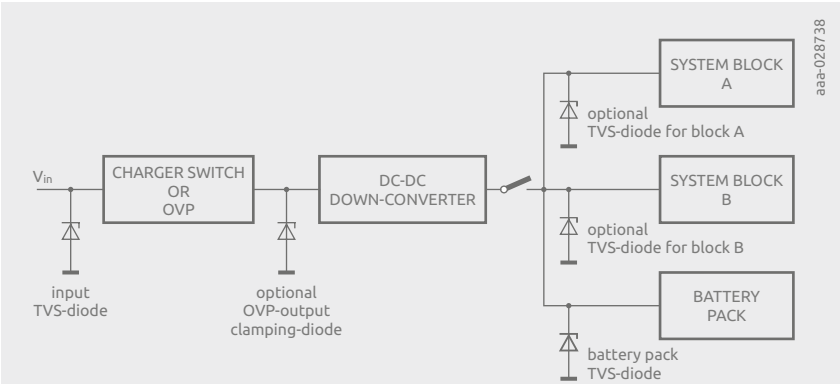

Figure 75 | Example of a charger path with protection diodes at typical locations

7.8.5 USB as a power input

For many applications in the consumer technology sector, USB has become the standard port to supply devices with power, regardless of USB data functionality. While most use the USB port to provide the default 5 V/500 mA input, more power-hungry devices use the USB Power Delivery (PD) protocol to provide higher voltages and higher currents.

Figure 76 | Selection of USB-powered portable and stationary devices

Since its introduction in 2012, the USB power delivery specification has evolved over several revisions with ever increasing power ratings. Table 40 provides an overview of USB PD output currents, voltages, and power ratings.

Table 40: USB PD 2.0 and 3.0 source power rules

Source output power rating (W)		Current, at: (A)						
		+5 V	+9 V	+15 V	+20 V	+28 V[1]	+36 V[1]	+48 V[1]
Standard Power Range (SPR)	0.5–15	0.1–3.0	N/A	N/A	N/A	N/A	N/A	N/A
	15–27	3.0 (15 W)	1.67–3.0					
	27–45		3.0 (27 W)	1.8–3.0				
	45–60			3.0 (45 W)	2.25–3.0			
	60–100				3.0–5.0 [2]			
Extended Power Range (EPR)	100–140				3.0 (60 W), 5.0 (100 W)[2]	3.57–5.0		
	140–180					5.0 (140 W)	3.89–50	
	180–240						5.0 (180 W)	3.75–5.0

1) requires electronically marked EPR cables
2) requires electronically marked 5 A cables

The first revision (USB PD 1.0) defined six fixed power profiles spanning from 10 W to 100 W. USB PD 2.0 and 3.0 introduced more flexible rules, where inside fixed power and voltage brackets the negotiated current is more flexible. USB PD 3.0 also added communication features for checking battery condition, enhanced security and fast role switching. A major upgarde was introduced with USB PD revision 3.1, which extended the output power range to 240 W with the Extended Power Range (EPR). As for the 100 W mode of the Standard Power Range (SPR), the higher EPR voltages (28 V, 36 V and 48 V) require electronically marked cables to ensure that the cables can conduct the high currents without power losses becoming too high.

Protection devices for USB PD-enabled ports should always be chosen such that the maximum reverse working voltage, V_{RWM}, reflects the maximum V_{BUS} voltage which the device can negotiate to be supplied from the USB power supply. For the default 5 V V_{BUS} supply, protection devices with 5 V V_{RWM} are suitable. In the Nexperia nomenclature, these will be products of the PTVS5V0xxx family. Higher maximum V_{BUS} voltages of 9 V, 12 V and beyond will require 9 V or 12 V V_{RWM}. In Nexperia terms, the appropriate products are found in the PTVS9V0xxx or PTVS12Vxxx families, respectively.

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- "Road vehicles – Component test methods for electrical disturbances from narrowband radiated electromagnetic energy, Part 4: Harness excitation methods," Standard, International Organization for Standardization, Geneva, CH, 2020.
- Ethernet (Wikipedia), https://en.wikipedia.org/wiki/Ethernet

Chapter 8

Troubleshooting and system optimization

8.1 Latch-up analysis for deep-snap back devices

8.1.1 Introduction

Every new generation of data interfaces sees an increase in data rates. High-speed interfaces like USB 3.x can be found in almost all end-application areas, including computing and consumer applications. Due to electrification and introduction of enhanced safety and multimedia functionality there is a growing use of high-speed data communication in automotive products. Higher data rates require lower parasitic capacitances for the inputs of system chips, which also implies higher sensitivity of these inputs to surge and electrostatic discharge (ESD) events.

Additionally, sensitivity of digital interfaces has increased due to ongoing miniaturization of semiconductor structures.

For the design of robust systems capable of withstanding incoming ESD strikes, it has become mandatory to add external ESD protection devices. ESD protection diodes should be placed as close as possible to the entry point of an ESD strike. If the protection device is located close to the connector of an external interface, overvoltage pulses are shorted to ground directly at the connector. Less current can flow into the entire PCB and into the system chip, or lead to malfunction via an unexpected current path on the board. Finally, the available line inductance will reduce the peak clamping voltage, while the line resistance will slightly limit the current flowing into the protected system if most of it is located between the ESD protection device and protected system in the PCB layout.

To solve this problem, high performance ESD protection devices have to be selected which combine a very low capacitance, to maintain the signal integrity of the digital signals, with good clamping capability that clips the residual voltage of a surge event into the allowed range of the interface to be protected. The most important topologies for ESD protection devices are discussed in Chapter 3 of this Guide.

The lowest clamping voltages are possible with deep snap-back devices. For these devices, it is necessary to investigate carefully whether there is a risk of ending up in a latch-up condition if an ESD strike triggers a snap-back protection device.

Deep snap-back devices show a very low leakage current below the stated operating voltage V_{RWM}. If the voltage is increased, current becomes higher. At a specific voltage, V_{t1}, the component turns on and voltage across the device falls significantly. With further increase of current the clamping voltage increases with a preferably steep I-V curve, so a low dynamic resistance. If current through the diode is reduced, the device snaps back into a high-ohmic state if it falls below a specific hold current or hold voltage. In Figure 1, a typical I-V characteristic of a deep snap-back ESD protection diode is depicted. At about 7.7 V the device turns on and jumps down to about 1.3 V. If current becomes smaller than the hold current I_{HOLD} of about 22 mA the device returns to off state. V_{HOLD} is about 2.4 V. Like a thyristor, such ESD protection shows a hysteresis in the I-V curve, so turn-on happens at a higher voltage and current compared to the turn-off. The device depicted in Figure 1 has a symmetrical I-V characteristic (only the positive polarity region is shown here). For the clamping voltage the equation below can be applied above the snap-back voltage:

$$V_{clamp} = V_{snapback} + R_{dyn} \cdot I_{PP}$$

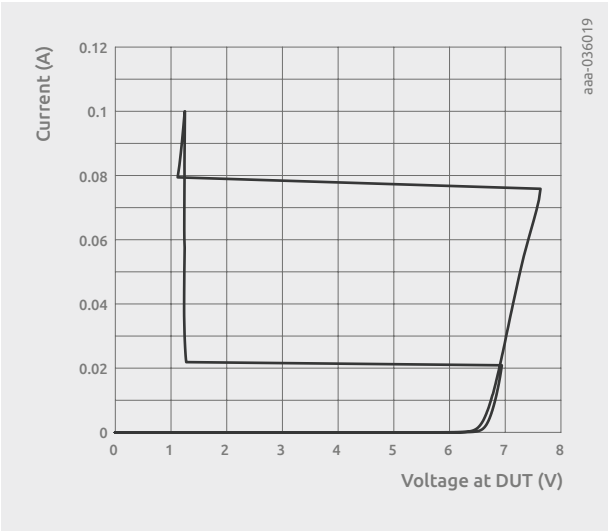

Figure 1 | I-V characteristic of a deep snap-back ESD protection device

The snap-back characteristic can also be seen in a transmission line pulse (TLP) curve. Figure 2 shows the TLP curve of the same component used for Figure 1. The hold current cannot be derived from a TLP curve, but from the test results of an I-V curve tracer or a similar test approach. In a TLP curve test, pairs of voltage and current from several TLP pulse shots with increasing voltage are recorded as a special I-V curve. A TLP curve shows the snap-back voltage accurately but neither an exact hold voltage nor the hold current. For a device with a high trigger voltage, TLP current at the snap-back can be quite high, much greater than the hold current with:

$$I_{trigger} = \frac{128\ V - 7.5\ V}{50\ \Omega} = 106\ mA$$

The hold current I_{HOLD} for a DC condition can be derived from the bottom left corner of the hysteresis curve depicted in Figure 1 only. In this application note we will show that the hold current, required to keep the protection device in on-state for an AC-operating mode, can be significantly higher than the DC value.

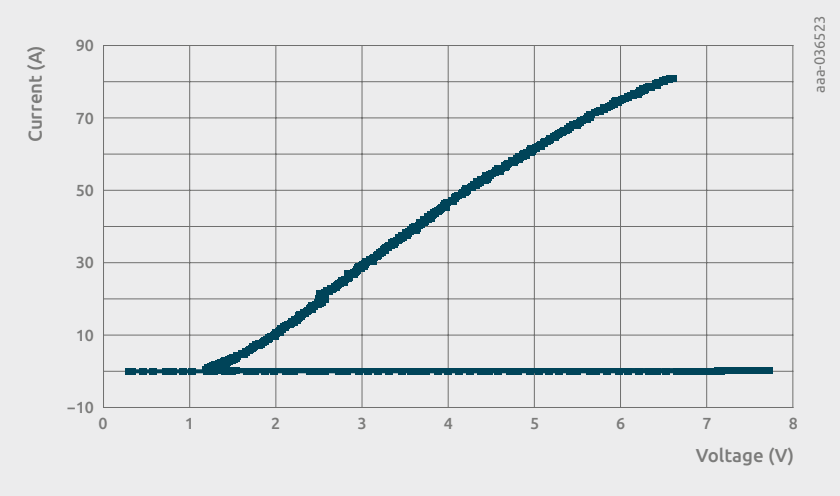

Figure 2 | TLP curve of a deep snap-back ESD protection device

8.1.2 Load line analysis approach

For deep snap-back devices, the application has to be reviewed if there is a risk that the ESD protection device remains in on-state after a surge event has passed. This is a so called 'latch-up' condition, where a circuit does not return to normal operation mode after a trigger event has happened.

Deep snap-back devices are not applicable for DC supply lines. DC supplies can easily provide hold currents of typical deep snap-back ESD diodes. After a deep snap-back ESD diode has been triggered, a DC-supply would drive the maximum output current through the ESD diode, and it is likely that the protection device will be damaged by an electrical overstress (EOS) failure, because the maximum allowed junction temperature will be exceeded.

For data interfaces the situation needs to be evaluated in more detail. The current drive capability of the driver stages is limited to lower currents than in the supply voltage scenario described above. Maximum current is the result of the open-loop source voltage and the driver output resistance, which is often predefined by the standard termination of an interface.

With a load line analysis, latch-up scenarios can be evaluated using a graphical approach. In Figure 3 the load line of an output is depicted in red for a voltage source or a driver stage with a voltage of V_{BUS} and an output resistance of R_S. Maximum output current is present if the output is shorted.

$$I_{SHORT} = \frac{V_{BUS}}{R_S}$$

If no current must be provided the open loop voltage V_{BUS} is present at the driver output.

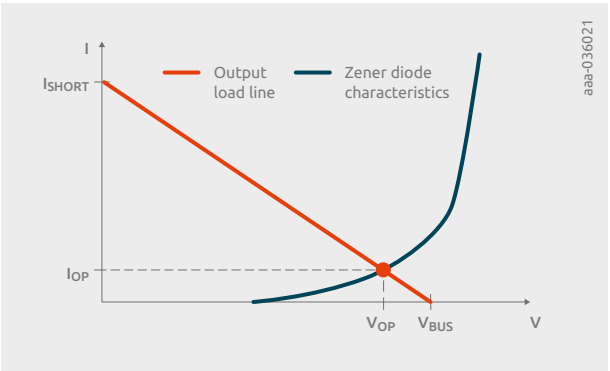

Figure 3 | Load line principle (output load line in red, Zener diode characteristic in blue)

The load line is a linear curve (red line) starting from I_{SHORT} and V_{OUT} = 0 V, with $I_{SHORT} = \frac{V_{BUS}}{R_S}$ going down to the point with I_{OUT} = 0 A and $V_{OUT} = V_{BUS}$.

An I-V characteristic of a Zener diode is overlaid in blue. For the circuit shown in Figure 4 which is a Zener diode with the assumed blue non-linear I-V curve connected to the voltage source V_{BUS} and the output resistance R_S, the intersection of the two curves is the operating point, which fulfills the equation:

$$V_{OP} = V_{BUS} - R_S \cdot I_{OP}$$

Only one operating point or intersection is possible. A latch-up is impossible with an ESD protection like a Zener diode. Leakage current in the working voltage area is very low and the breakdown voltage is not exceeded in normal operation ($V_{BR} > V_{BUS}$).

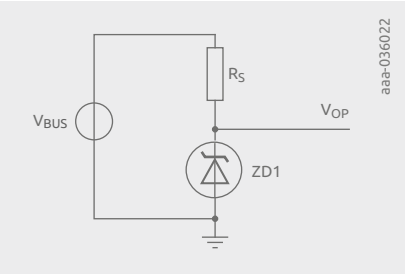

Figure 4 | Voltage source with series resistor R_S and Zener diode ZD1 as load

In Figure 5 the I-V curve of a snap-back ESD protection device is overlaid with the linear load line of a voltage source and a series output resistor as depicted in Figure 8. There are now two intersections between the two curves, or in other words two possible stable operating points. In normal operation an interface stays below the trigger voltage, at the operating point OP1. An ESD strike can move the operating point to OP2. The voltage V_{OP2} is very low because of the deep snap-back voltage in on-state of the ESD protection. If the interface driver continues to work with the red load line set-up the interface is stuck in a latch-up condition. The signal line can no longer change the single-ended state.

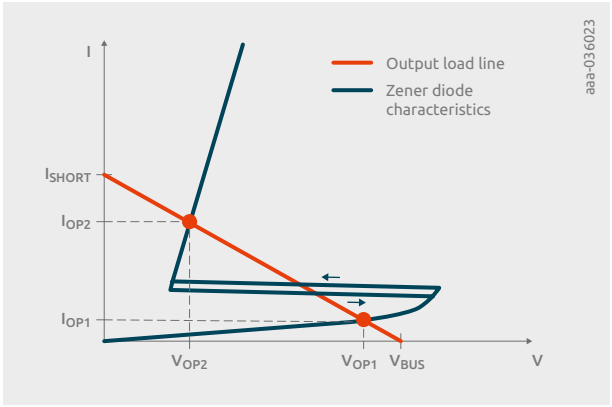

Figure 5 | Load line of a voltage source with series resistor R_S and an overlaid I-V curve of a snap-back ESD protection

The scenario depicted in Figure 6 has no risk of latch-up. After a surge event the hold current of the snap-back ESD diode cannot be provided and the interface can return to normal operation.

To safeguard this there are several options. An ESD diode with a suitable hold current can be selected. Another solution is to make the load line flat enough to avoid multiple intersections. This can be achieved with a smaller ISHORT addressed with a higher resistance in the output of the driver stage or a smaller single-ended high state drive voltage. The latter options are more

of a theoretical nature because standard high-speed interfaces have fixed electrical definitions in terms of termination and voltage levels.

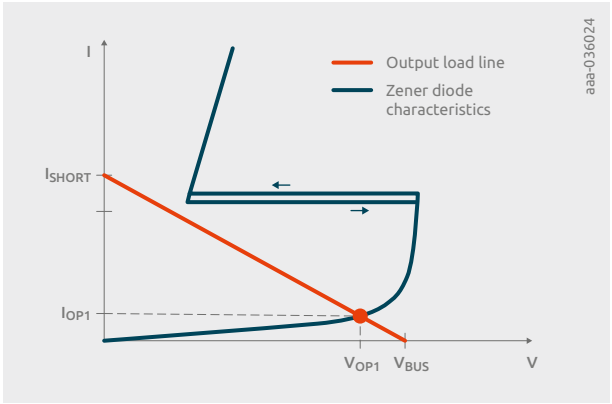

Figure 6 | Snap-back device combined with a latch-up free load line situation

DC supplies usually have a very low R_S which means that the output maintains an almost constant voltage with no dependence on the output current in the ideal case. For V_{OP1} greater than V_{HOLD} a latch-up will occur and the ESD protection device will be damaged by electrical overstress (EOS) likely. For safe operation the relationship $V_{HOLD} > V_{DC}$ must be obeyed as shown in Figure 7.

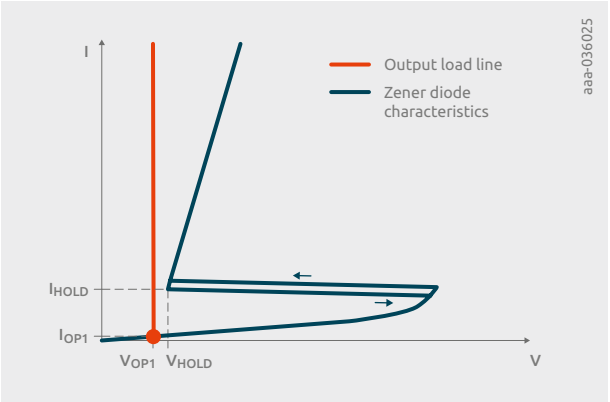

Figure 7 | Snap-back device combined with a latch-up free load line situation

An example of an AC signal protected with bi-directional snap-back ESD protection is shown in Figure 8. The ESD protection device turns off again after a polarity change and normal operation can continue in the voltage area below the trigger thresholds within the stated V_{RWM} range where leakage current is extremely low.

For high-speed data signals the drivers do not output a constant logical state. Modern interfaces are coded such that the digital 0 and 1 states appear for an identical number of clock cycles. This has the significant advantage that the signal is DC-free and can be coupled via capacitors.

According to the load line approach a snap-back ESD diode should turn off with the next single-ended low state for an ideal component. In Figure 9 it is assumed that the low state voltage is 0 V.

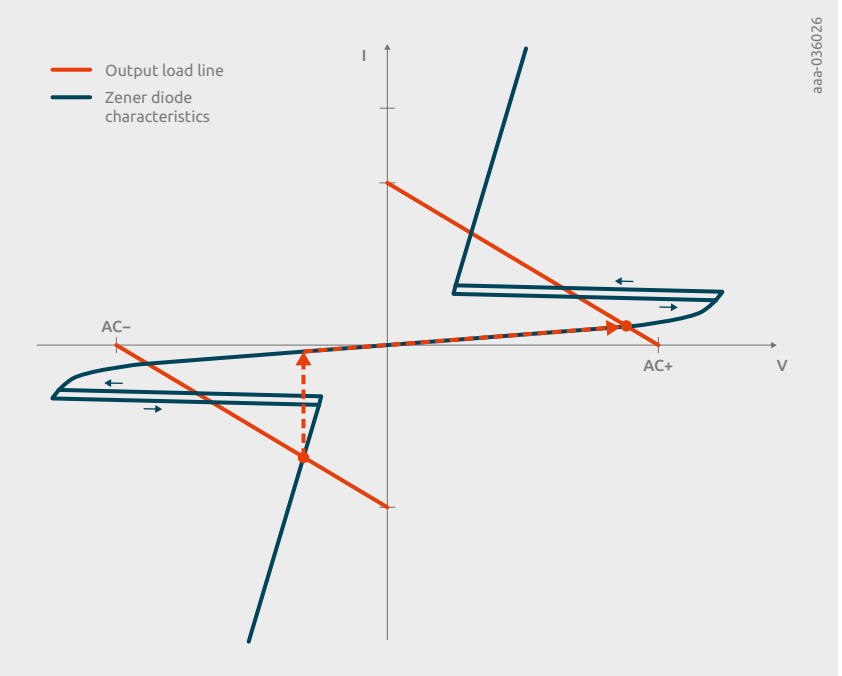

Figure 8 | Bi-directional snap-back device applied to an AC signal line. Recovery from on-state to high-ohmic off-state after a negative ESD event (dotted red line) followed by a signal polarity change

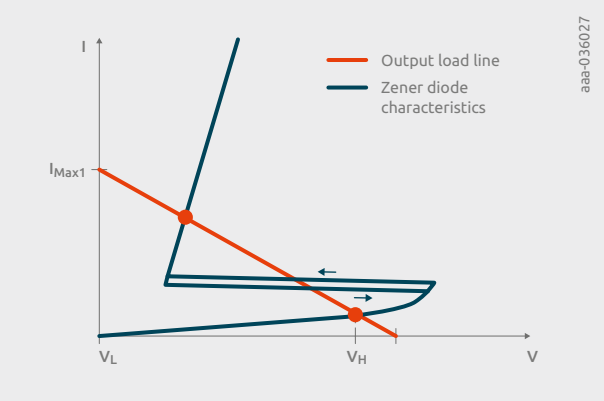

Figure 9 | Example of high to low state change of a single-ended data line

8.1.3 Turn on and turn off behavior at a high frequent signal line

For deep snap-back devices, the application has to be reviewed if there is a risk of the ESD protection staying in on-state or a latch-up condition.

If a snap-back ESD diode is connected to a function generator which outputs a rectangular signal with a frequency equal to or higher than 5 MHz at a duty cycle of 50%, the signal level can be increased until the protection device turns on once the trigger level is reached or exceeded. The simple test setup is shown in Figure 10. Snap-back ESD protection components are designed such that they turn on extremely quickly. A low clamping voltage is required almost instantaneously to provide effective protection against incoming surge events. If the generator is adjusted to 12.8 V output voltage, the snap-back device is turned on and stays in on-state because the average hold current is high. The part does not turn on and off with every clock cycle. The pulses applied are clamped down to about 1.4 V as shown in Figure 11. This snap-back voltage for the example device can also be seen in Figure 1 and Figure 2 in Section 8.1. The voltage at the DUT is about 7.5 V before the device snaps back. The pulse trigger current is:

$$I_{trigger} = \frac{12.8\ V - 7.5\ V}{50\ \Omega} = 106\ mA$$

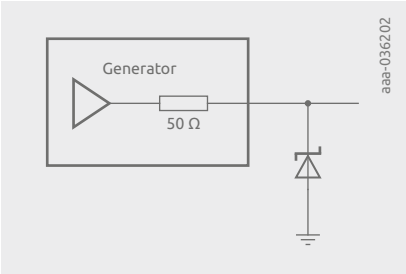

Figure 10 | Test set-up with rectangular signal applied to DUT

Figure 11 | Turn on of snap-back ESD protection in 5 MHz signal. The green trace shows a reference signal which is not clamped. The red trace is the clamped signal at the ESD protection diode.

If the generator voltage is decreased step by step, the protection device turns off at an adjusted generator voltage of about 9.3 V. This operating point is the hold condition where the device leaves the deep snap-back.

For $I_{pulse(hold)}$ it can be stated:

$$I_{pulse(hold)} = \frac{V_{generator} - V_{clamp}}{50\ \Omega} = \frac{9.3\ V - 1.4\ V}{50\ \Omega} = 158\ mA$$

From this hold condition operating point, the clamping voltage jumps up from the snap-back voltage to about 7.1 V, which is roughly the bottom right corner of the hysteresis curve shown in Figure 1. The pulse current can be calculated with the formula:

$$I_{pulse} = \frac{V_{generator} - V_{clamp}}{50\ \Omega} = \frac{7.1\ V - 1.4\ V}{50\ \Omega} = 114\ mA$$

This scenario, where the device has just turned off, is depicted in Figure 12.

With the turn-off and the jump back to a higher clamping voltage (7.1 V for the device discussed here), the throughput current falls and the generator voltage needs to be increased as it is in the turn-on experiment to return to snap-back. So a significant hysteresis can be observed. The operating point seen after the snap-back is released would not normally be reached in a real high-speed interface because the drive voltage is around 7.1 V. The ESD diode would return to the full high-ohmic state directly, which means the interface would return to the V_{RWM} voltage range following an ESD strike.

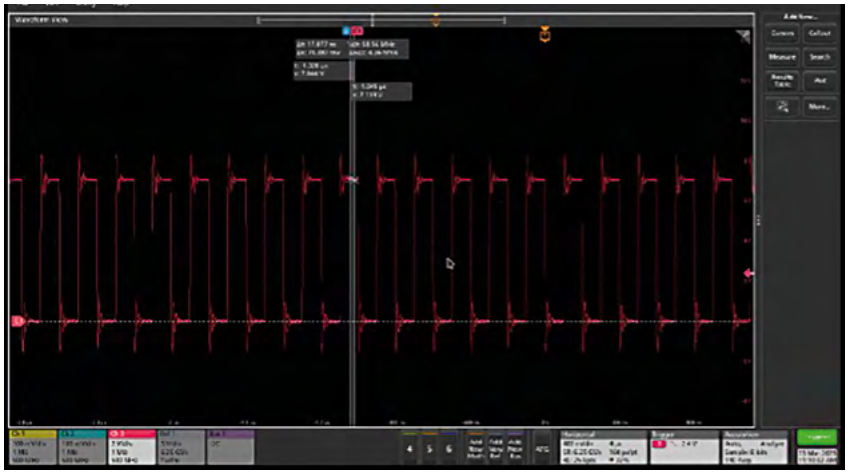

Figure 12 | Turn off

With further reduction of the generator voltage, eventually almost no current flows, as would be expected from an I-V curve like the one depicted in Figure 1. From a generator voltage of 7 V and below this high-ohmic state is reached. The diode voltage is identical to the adjusted generator voltage.

In Figure 13 a hysteresis curve is shown which is valid for the described 5 MHz test. The hold current for the pulses is much higher compared to the DC-test hysteresis curve shown in Figure 1. The pulses need a higher current to create an average current high enough to keep the snap-back device in on- state.

Figure 13 | I-V-hysteresis curve of a Treos ESD protection device. 5 MHz test signal with 50 Ω output resistance of the signal generator

The takeaway from this experiment is that the risk of a latch-up can be significantly reduced for deep snap-back devices if a high-speed digital data signal is applied. From about 5 MHz upwards, snap-back protection devices can be kept in a constant on-state if the pulse amplitude is high enough. This means that the devices do not turn off after each high state of a data signal. To keep a latch-up active, the high state pulses need a higher hold current than the I-V curves would suggest. The hold current needed per pulse is similar to the trigger current. The described test has been performed applying ground level as the low state of the signal. The effect of a relaxed latch-up risk becomes fully effective if there is no bias voltage overlay.

USB legacy mode signals such as USB LS and FS modes or open-drain bus signals can benefit from this knowledge.

8.1.4 Latch-up considerations for major data interfaces

USB Interfaces

For USB interfaces the USB 2.0 data lines D+/D- operate in half-duplex mode. This means the direction of data may change sequentially on one differential pair. For USB 3.x and USB 4 there are separate signal pairs for data flow directions allowing full-duplex operation of the interface.

The D+/D- lines for USB 2.0 and the super-speed data lines RX+/RX- and TX-/TX+ have a different realization in hardware and need to be discussed separately with respect to a risk of latch-up in combination with SCR-based ESD protection devices.

USB 1.1 (LS)/(FS) and USB 2.0 (HS) data lines

In Figure 14 a block diagram of an USB 2.0 transceiver is shown. There are two driver stages connected to the data lines. The LS/FS driver supports the legacy Low-speed (LS) and Fast-speed (FS) modes of USB 1.1.

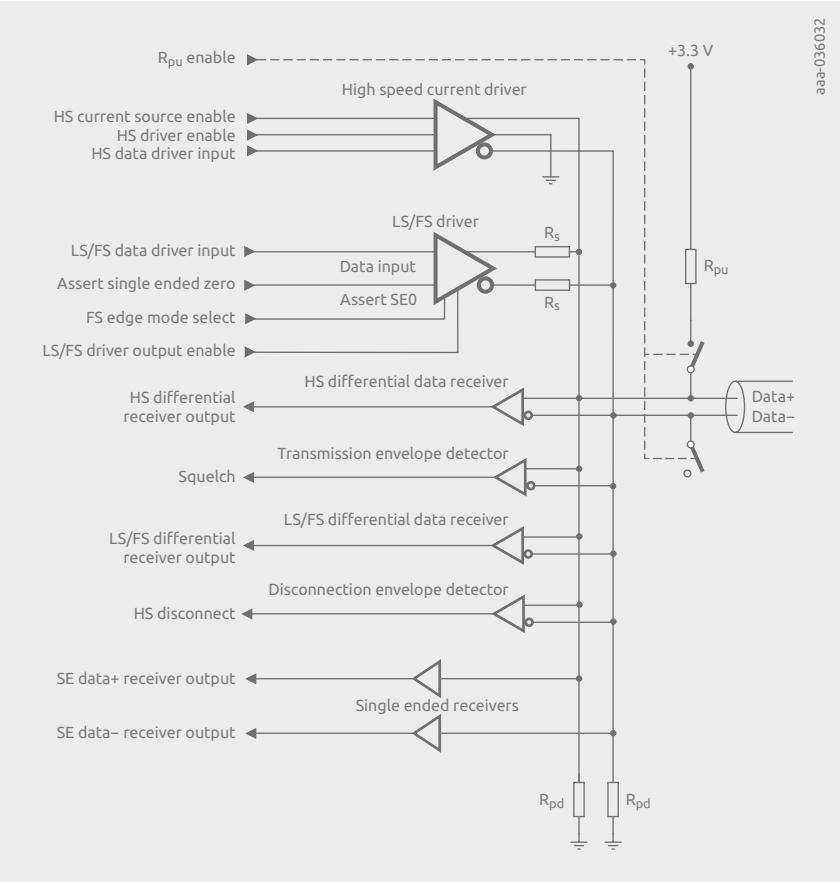

Figure 14 | USB 2.0 transceiver block diagram with LS/FS and HS drivers

Detection of the data speed capability of a device connected to a host is performed by connecting a 1.5 kΩ pull-up resistor Rpu to the D- line for LS mode as shown in Figure 15 or to the D+ line for FS mode as shown in Figure 16. A USB 2.0-capable device must have a pull-up resistor at the D+ line. The bit rate is 1.5 Mbit/s for the low-speed mode and 12 Mbit/s for fast-speed mode.

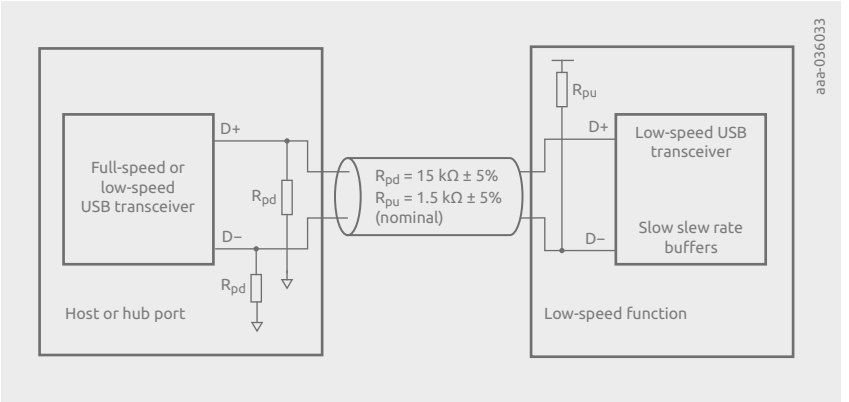

Figure 15 | Low-speed system, Rpu placement at D- line

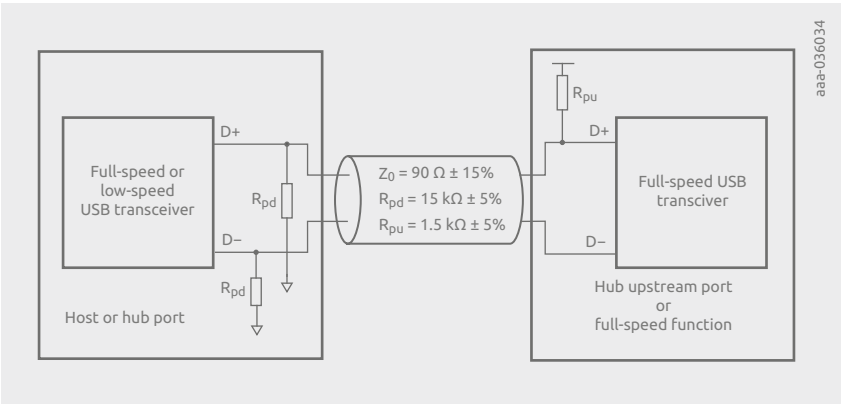

Figure 16 | Full-speed system, Rpu placement at D+ line

A USB 2.0 host uses a so called chirp sequence if the connected device can communicate in high-speed (HS) mode. In Figure 17 the procedure is shown in detail. The host starts a reset with the LS/FS drivers terminating both series resistors R_S to ground. HS drivers work with 17.78 mA current sources to generate a high state on a signal line. After the host's grounding of both signal lines, a connected USB 2.0-capable device sends a K-state with its HS-driver for at least 1 ms. The high level is 800 mV. The hub then answers with K_J chirps. After this the device disconnects the pull-up resistors and connects the R_S series resistor to GND. The level of the single-ended signals is decreased to 400 mV nominal with the final USB 2.0 termination scheme.

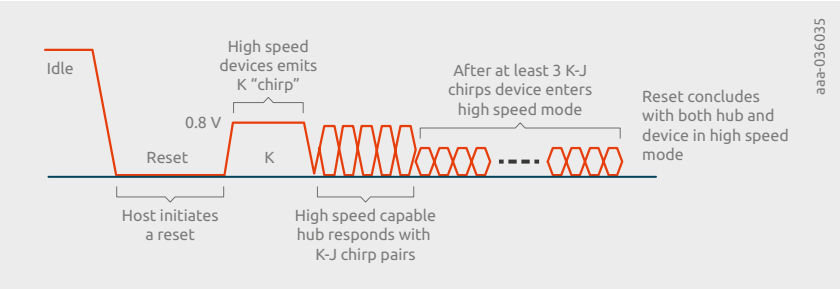

Figure 17 | USB 2.0 "Chirp" sequence

A simplified schematic for calculating the maximum latch-up current supplied from an LS/FS driver is shown in Figure 18. The 15 kΩ pull-down resistors are present at downstream-facing transceivers only on both signal lines of the D+/D- lane, whereas the pull-up resistors are placed at one signal line only as explained above. These pull-down and pull-up resistors can be neglected for the latch-up current calculation because the series resistor R_S is much smaller with a value range from 28 Ω to 44 Ω for a device without USB 2.0 capability. The nominal high state voltage at the driver is 3.3 V. The maximum allowed voltage is 3.6 V. For the latch-up risk assessment the worst case scenario must be considered with 3.6 V drive and the smallest allowed series resistance of 28 Ω. For a system which is capable of USB 2.0 the series resistors need to fulfill the requirement for R_S of 45 Ω ±10%. The worst case is 40.5 Ω.

The maximum current through a snap-back ESD protection device in on-state to be considered in an LS/FS system is:

$$I_{ESD\ diode} = \frac{3.6\ V - V_{snapback}}{28\ \Omega}$$

For a USB 2.0-capable device, the formula to be applied is:

$$I_{ESD\ diode(max)} = \frac{3.6\ V - V_{snapback}}{40.5\ \Omega}$$

The USB LS/FS modes benefit from the finding, discussed in Section 4, that deep snap-back devices require a higher hold current for data signals with more than about 10 Mbit/s compared to hold currents derived from a DC-based I-V curve measurement. This reduces the latch-up risk significantly.

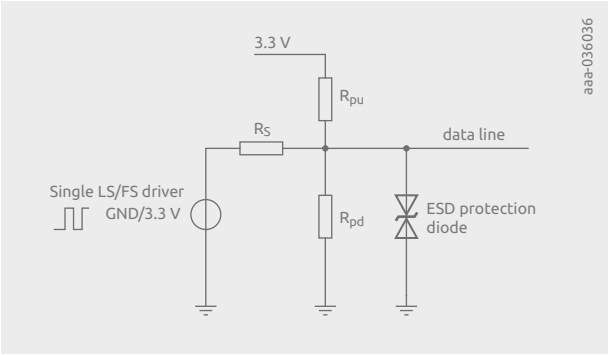

Figure 18 | LS and FS driver schematics with termination and ESD protection diode. Rpd is present at downstream-facing transceivers, Rpu at upstream-facing transceivers

In Figure 19 a simplified schematic diagram for a connected USB 2.0 system in HS mode is depicted.

The driver stage is a switched-current source with 17.78 mA nominal high state current. Host and USB device are connected via a USB cable. The parasitic components of the cable are neglected. On both sides a 45 Ω termination to ground is provided via the LS/FS drivers (see Figure 14).

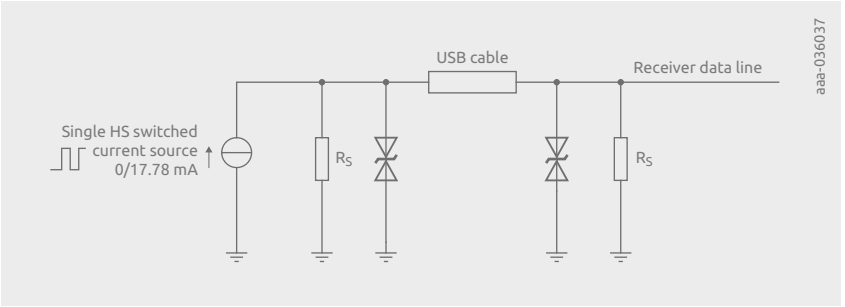

Figure 19 | HS driver schematic diagram with 45 Ω termination at host and device side and a switched-current source as driver output stage

The nominal single-ended high state voltage is then V_{OH} = 17.78 mA x 22.5 Ω = 400 mV. As worst case for latch-up risk, the maximum driver current combined with the maximum resistance must be considered. The USB 2.0 specification allows a 10% tolerance. $R_{S(max)}$ is 49.5 Ω and the maximum current is 19.56 mA, meaning that the maximum high state voltage is about 500 mV.

In Figure 20 this equivalent worst-case scenario with a converted current source to a voltage source is depicted.

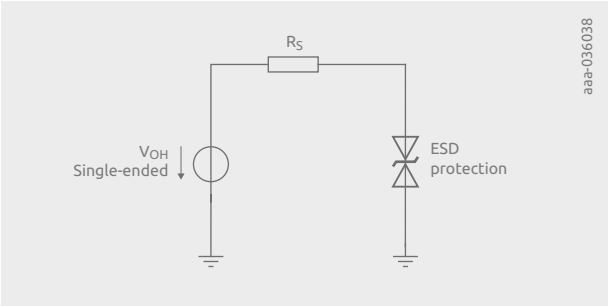

Figure 20 | Equivalent HS driver with converted voltage source for latch-up evaluation

Based on the facts discussed above, it can be concluded that a latch-up in LS and FS mode can happen in a connected condition with a shielded USB cable only, because the LS/FS drivers become active after connecting and after the location of Rpu has been sensed. It is very unlikely that an ESD strike can enter the system after connection is established. This means the risk of a latch-up issue for D+/D- data lines is usually very low.

For the residual surge risk at a connected link in a USB 1.1 system, a hold voltage above 3.6 V is safe, or if hold current is above the maximum possible high-state current for the ESD diode according to the above given formula for the maximum allowed current of an USB 2.0-capable device. If we assume a $V_{snapback}$ of 2 V as an example, I_{HOLD} should be higher than 39.5 mA.

For a USB 2.0 system, the low maximum drive voltage eliminates the risk of a latch-up if the snap-back voltage is higher than 0.5 V. This is the case for all major deep snap-back ESD devices on the market.

USB 3 and USB 4 data lines

With the super-speed USB interface, signals are transmitted via at least one pair of separate RX and TX lanes. This allows full-duplex operation which means that sending and receiving data at the same time is supported. The USB Type-C connector is becoming the mainstream connector type, increasingly replacing older connectors like Type-A, mini and micro connectors more and more. The Type-C connector provides two TX signal pairs as well as two RX pairs. In Table 1 the evolutionary increase of the data rate can be seen with the introduction of new modes. The mode names have been changed to a common nomenclature and now indicate more clearly which lane speed is applied and how many lanes are used.

Table 1: Overview of USB super-speed modes

Mode Name	Old name	Number of lanes	Lane Speed (Gbit/s)	Nominal interface speed (Gbit/s)
USB 3.2 Gen 1x1	USB 3.0 or USB 3.1 Gen 1	1	5	5
USB 3.2 Gen 1x2		2	5	10
USB 3.2 Gen 2x1	USB 3.1 Gen 2	1	10	10
USB 3.2 Gen 2x2		2	10	20
USB 4 Gen 2x1		1	10	10
USB 4 Gen 2x2		2	10	20
USB 4 Gen 3x1		1	20	20
USB 4 Gen 3x2		2	20	40
USB 4 Gen 4x1		1	40	40
USB 4 Gen 4x2		2	40	80

Whereas USB 3.2 Generation 1 (Gen 1) supports 5Gbit/s, USB 3.2 Generation 2 (Gen 2) offers 10 Gbit/s. The number of lanes appears after the x in the mode name. With two lanes the overall data rate of the interface is doubled nominally. With USB 4 even higher data rates are introduced. Generation 3 is associated with 20 Gbit/s lane speed and Generation 4 with 40 Gbit/s. The maximum nominal interface data rate in a combination of Gen 4 and two lanes is 80 Gbit/s.

In Figure 21 the topology of USB super-speed lines RX and TX is depicted.

From USB 3.2 Gen 2 x1 (previously USB 3.1 Gen 2) onwards the receiver inputs are AC-coupled with 330 nF capacitors. The signal lines in the cable have no bias voltage provided from the SoC inputs. In case of short circuits to V_{BUS} at the connectors or in the cables, the DC voltage cannot become present constantly at the RX input pins but stresses the input for a limited time while the coupling capacitor is charged.

With the ESD protection placed as depicted in Figure 21, there is no risk of latch-up because no DC bias is possible due to the coupling capacitors if there are no short circuits to V_{BUS} in a severe fault condition. The placement of the ESD protection at the connectors has the additional advantage that the capacitors are protected against ESD strikes. This can be important for small package capacitors which can be sensitive to very high current from ESD events. The charge from surge events increases the voltage of the capacitors, which can exceed the specified limit if multiple strikes are applied.

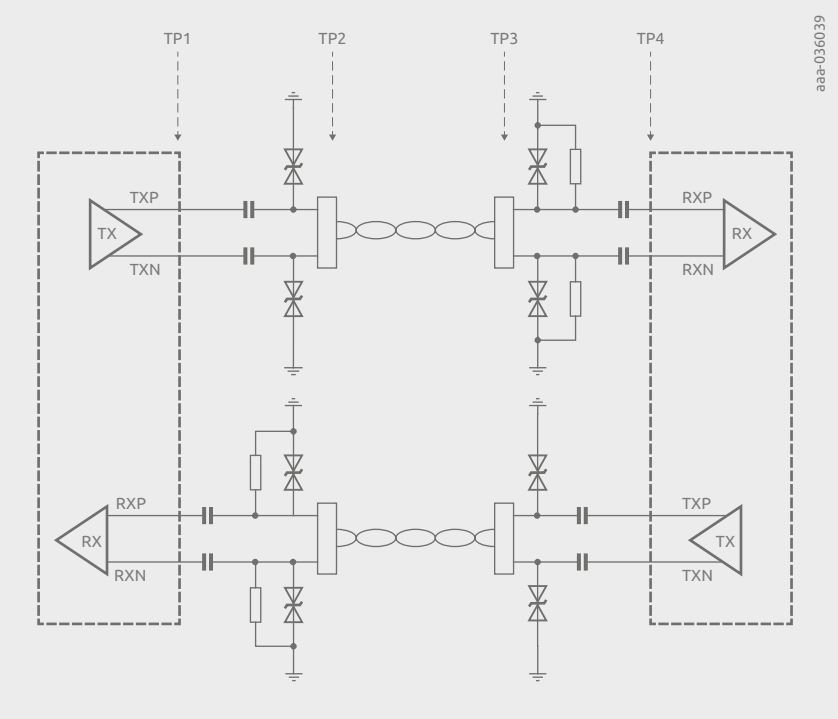

Figure 21 | Interface topology for USB super-speed signals RX and TX

If ESD protection is placed directly at the TX Phy-Output the possible voltages and currents for this scenario have to be evaluated. In the USB 3.2 revision 1.1 specification document, waveforms for single-ended and differential signals on the TX-lines are depicted as shown in Figure 22. For the maximum possible single-ended voltage the maximum differential voltage as well as the maximum common mode or bias voltage must be considered. $V_{TX\text{-}DIFF\text{-}PP(max)}$ is 1.2 V. $V_{CM(max)}$ is 2.2 V.

$$\frac{V_{TX\text{-}DIFF\text{-}PP(max)}}{2 + V_{CM(max)}}$$

Maximum single-ended voltage has to be expected as worst case. The nominal termination is 45 Ω. The termination ranges from 36 Ω to 60 Ω. For latch-up considerations the minimum resistance of 36 Ω defines the worst-case scenario.

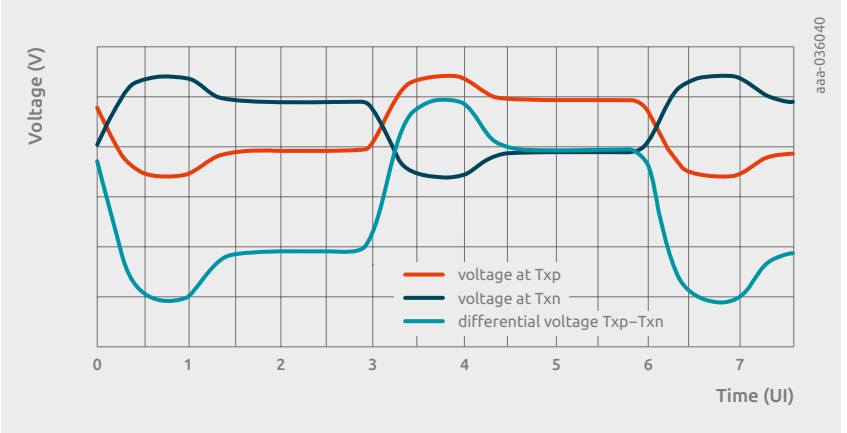

Figure 22 | Single-ended and differential voltage waveforms for TX lines

Maximum latch-up current at the SoC TX pin can then be:

$$I_{(max)} = \frac{2.8\ V - V_{snapback}}{36\ \Omega}$$

Placing the protection behind the coupling capacitors is not inherently safe against a potential latch-up.

As stated above, placing the ESD protection at the cable connectors is completely safe regarding latch-up if two capacitors per data signal are present as shown in Figure 22. If there is no coupling capacitor at the super-speed inputs at the Phy in a legacy implementation of USB 3 there is one more scenario to be considered.

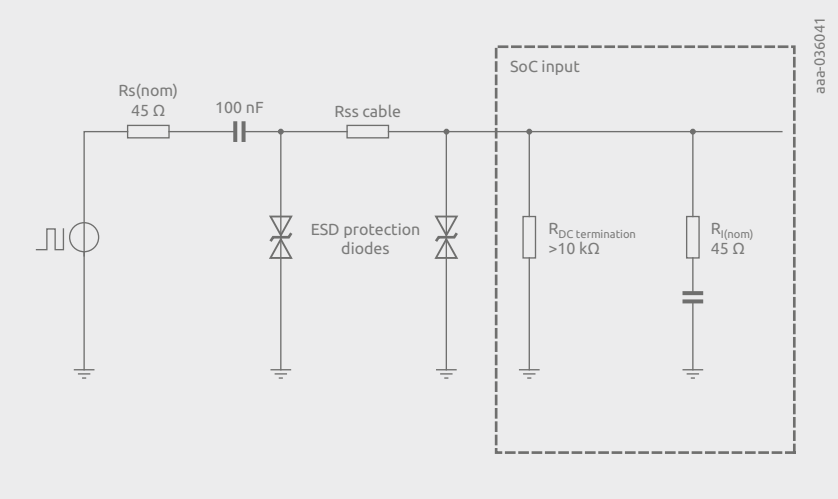

Figure 23 | Equivalent circuit diagram for super-speed signal path from TX to RX input without capacitive coupling at RX SoC pin

Figure 23 shows the equivalent circuit diagram. The data signal is driven via R_S. ESD protection is assumed at the transmitter as well as at the receiver side. The receiver input has a DC termination of more than 10 kΩ. Therefore, no significant and constant latch-up current can flow. This scenario has no latch-up risk.

In conclusion, USB 3 and USB 4 are safe against latch-up risk; only a protection of the TX-pins at the SoC behind the coupling capacitors requires attention.

8.1.5 HDMI interface (TMDS lines)

HDMI (High-Definition Multimedia Interface) is the major digital interface in the market for audio/video connections. Later generations include Ethernet and 3D features. CEC (Consumer Electronics Control) allows connected devices to control each other: for example, a TV can start a connected media player once the related input has been chosen. HDMI also supports HDCP copy protection, which protects content against unauthorized copying. Resolution has been increased continuously in terms of quantization as well as in supported color spaces. This has led to an increase of data rate as for the USB interface described in the previous section.

7680 x 4320 progressive with 60 Hz frame rate is the highest resolution for HDMI 2.1 with 48 Gbit/s total data rate. The additional clock signal channel has been removed, and this lane is used as an additional data channel. Table 2 gives an overview of the different versions of HDMI.

Table 2: Overview of HDMI standards

HDMI version	1.0	1.1	1.2	1.3	1.4	2.0	2.1
Maximum pixel clock rate (MHz)	165	165	165	340	340	600	no extra clock channel
Maximum TMDS/FRL bit rate per lane including 8b/10b coding overhead (Gbit/s)	1.65	1.65	1.65	3.4	3.4	6	12
Maximum total TMDS/FRL throughput including 8b/10b coding overhead (Gbit/s)	4.95	4.95	4.95	10.2	10.2	18	48
Maximum audio throughput bit rate (Mbit/s)	36.86	36.86	36.86	36.86	36.86	49.152	49.152
Maximum video resolution over 24 bit/pixel single link	1920×1200 p/60 Hz	1920×1200 p/60 Hz	1920×1200 p/60 Hz	2560×1600 p/60 Hz	4096×2160 p/30 Hz	4096×2160 p/60 Hz	7680×4320 p/60 Hz
Maximum color depth (bit/pixel)	24	24	24	48	48	48	48

HDMI TMDS lines

HDMI signal lanes use transition-minimized differential signaling (TMDS). A current source driving 10 mA is connected to the TMDS+ or TMDS- line. At the receiver side 50 Ω pull-up resistors are connected to 3.3 V. The nominal differential termination is 100 Ω.

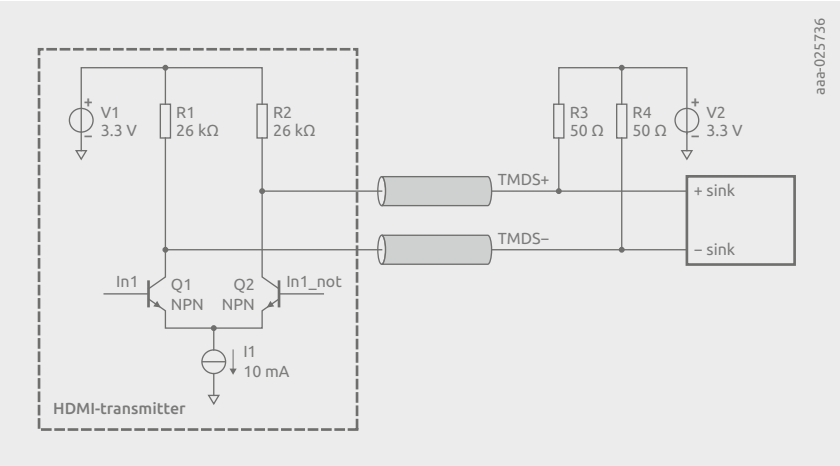

Figure 24 | Structure of TMDS signal path from transmitter to receiver

DVI interfaces have the same structure, and the conclusions described in this chapter are valid for DVI as well. For the evaluation of a latch-up risk the minimum resistance of the receiver termination must be considered. The nominal 50 Ω may deviate by ±10%. The pull-up resistors have a minimum resistance of 45 Ω. The supply for the pull-up resistor can be 5% higher than nominal which is a worst-case condition.

Latch-up current can be calculated with the equation:

$$I_{(max)} = \frac{3.465\ V - V_{snapback}}{45\ \Omega}$$

An HDMI interface requires some attention with respect to possible latch-up conditions. Many HDMI input circuits are designed with active silicon circuits for the 50 Ω pull-up resistors. HDMI interfaces have to be safe for short-circuits on the TMDS lines according to HDMI standard requirements. To avoid overheating of active pull-up resistors, the pull-up voltage is removed whenever a short is detected at the TMDS lines. This mechanism releases a latch-up condition. Note that TMDS lines begin data transfer after connection has been established. The risk of ESD strikes is much higher during the connecting process of a cable, and very unlikely to happen when connection is fully established. In practice, no known field returns are caused by latch-up failures with HDMI interfaces. If the formula for the maximum possible latch-up current is taken into consideration using an ESD diode with a higher I_{HOLD} any small residual risk of a hang-up is avoided.

8.1.6 DisplayPort

DisplayPort is popular in computing applications to provide a digital interface between a computer and a monitor. DP connections are offered as an option together with HDMI interfaces. Like HDMI, data rate is increasing with newer standards. DP 2.0 can support up to 77.73 Gbit/s on four parallel data pairs. As a video standard this is 7680 × 420 pixels with 60 Hz frame repetition rate and 12-bit resolution. Figure 25 shows the topology of a single data lane. At the TX- and RX-side the single lines are terminated with nominal 50 Ω against bias voltage supplies ($V_{bias\text{-}TX}$ and $V_{bias\text{-}RX}$). The transmitter side is AC coupled, whereas the receiver input pins are DC-connected to the DP-cable. The bias voltage can range from 0 V up to 2 V.

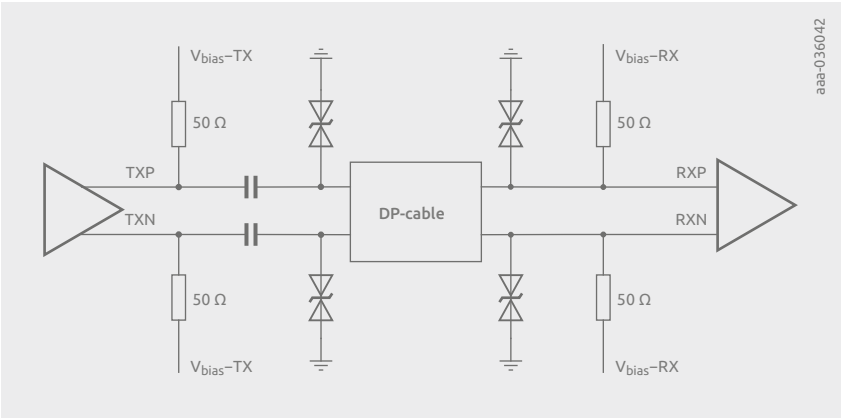

Figure 25 | Structure of DisplayPort data lane (four times present per data link)

Figure 26 shows an equivalent circuit for a single line of a DP interface. ESD protection is placed at the connectors of the DP source as well as the DP receiver. Without a connection, the RX side has no risk of a latch-up because of the AC coupling via capacitors. With a connected cable however the receiver side standalone has to be evaluated regarding a latch-up risk.

$$I_{(max)} = \frac{V_{bias-RX} - V_{snapback}}{50\ \Omega}$$

With ESD diodes that have a hold voltage above 2 V, the DisplayPort is safe against latch-up risk.

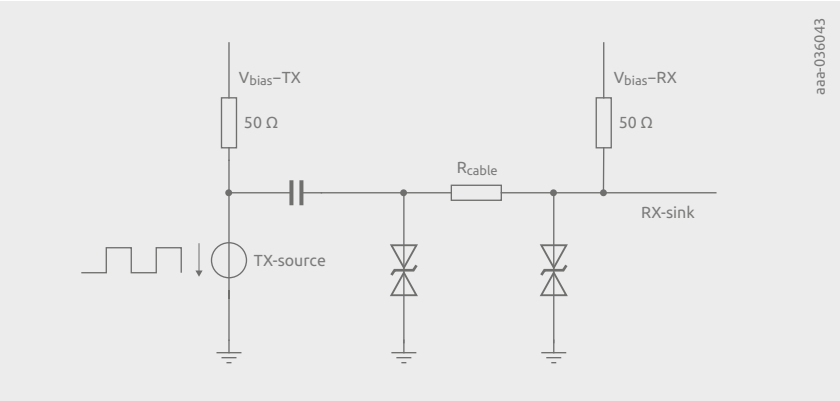

Figure 26 | Equivalent circuit of a single data line of DisplayPort

8.1.7 Conclusions

Modern high-speed interfaces require high performance ESD protection. A low clamping voltage must be achieved for incoming surge pulses. Dependent on the data rate of the target interface the capacitance of the protection diodes must be very small in a league 0.1 pF to 0.45 pF to avoid a big impact on signal integrity and the signal eye diagram. Snapback topology ESD protection has become the first-choice solution for sensitive interfaces. In the application note it was shown that the risk of latch-up can be managed well. For many scenarios like a USB 4 super-speed lane there is no latch-up risk because of capacitive coupling and the absence of a DC path to provide a hold current. In the other cases the selection of a suitable snapback voltage, hold voltage and current can eliminate the risk of latch-up. Very often there is a potential latch-up risk for an established data connection only. In normal handling of an interface, risk of a surge or ESD event is present when the connection gets established with connecting a cable where the

interface pin does not have a bias voltage yet to keep a snapback device in snapback mode. For higher signal frequency the effective hold current from the interface is not the same as for in a DC experiment due to an averaging effect. This reduces risk of latch-up compared to a simple calculation of maximum

single ended signal voltage. Consequently, snapback devices can be recommended as the most effective ESD protection solution for modern generation high-speed interfaces which can be found in retimers, redrivers, CPUs or PCI bridges for interface extensions

8.2 EMI scanner

In some troubleshooting situations, it is helpful to trace the ESD current to assess the layout of the PCB, the effects of the circuit or the effectiveness of the selected ESD diode and its position on the PCB. An EMI (electromagnetic interference) scanner can be an effective tool, particularly because it can visualize the currents and help to optimize the system.

EMI scanners are generally used in the frequency range to locate hotspots of active switching and emissions and to improve the PCB, housing and cabling. For ESD purposes, however, analysis in the time domain is more practical.

An EMI scanner like the one shown in Figure 27 consists mainly of a robot with a magnetic probe. A TLP source is connected to the DUT and emits a pulse to the MDI pins or another part of the PCB under test. The PCB under test is broken down into small pieces (typically 1 mm or less, depending on the size of the probe).

Figure 27 | EMI scanner for time domain ESD analysis.

The magnetic probe scans the surface to be examined by measuring the magnetic field at a certain distance (usually a few millimeters) above the PCB when a TLP pulse is applied. The scan is performed in both x and y directions to obtain two-dimensional magnetic field information. Once the entire area has been scanned, the information is merged and mapped. Surface currents are also calculated based on the magnetic field information [1].

Figure 28 shows an example of a visualized magnetic field distribution based on the 100 Base-T1 configuration described in Chapter 7.5. Based on the magnetic field, the engineer can see where most of the pulse energy flows when it enters the system through the connector. They can also assess which of the ESD protection strategies is the best when it comes to selecting the right electronic components and optimizing their placement on the PCB. The layout of the PCB can also be improved using this method.

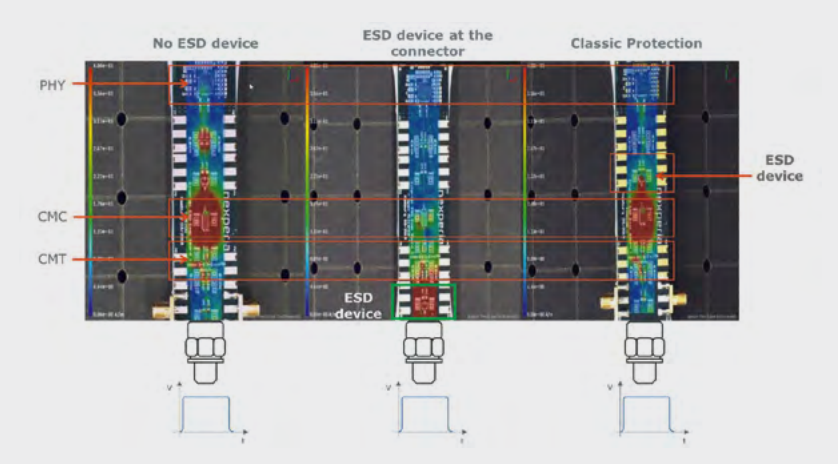

Figure 28 | EMI scanner results of a typical 100Base-T1 configuration (PHY, CMC, CMT and ESD device) and three different options of placing the ESD device on the PCM. The red color indicates a high magnetic field (directly related to surface current) and its distribution impacted by the placement of the ESD device.

There is another option of using an EMI scanner to test the robustness of the system by using an electric field probe (ESD probe). In this case, the DUT can be stressed by applying TLP pulses to different locations of the PCB, systematically checking the robustness of the system and, for example, the chip sets.

References

[1] A. P. Instruments, "API Technologies," Amber Precision Instruments, [Online]. Available: https://www.amberpi.com/index.php. [Accessed 17 07 2024].

Chapter 9

Device Modelling and Simulation

Device modelling is crucial to providing customers with a cost-effective and efficient way of finding the right product for their application and system. When it comes to ESD protection devices there are traditionally two main use cases to be considered. The first is the ESD behavior of the whole system including the full path from the external connector to the protected SoC, including external ESD protection, internal ESD protection, PCB and other discrete elements. The SEED approach described in Section 9.4 is a methodology that has been developed to perform this analysis.

The second use case is particularly needed when considering protection devices for data interfaces. Here, signal integrity (SI) needs to be investigated to ensure that the protection device does not harm the data transmission. For this use case, small signal SPICE models are generated. SI can also be checked using measured S-parameters, as explained in Section 6.1.

9.1 Small signal SPICE models (change Order SEED and ssSPICE)

The available models are based on product characterization and are generated independently of the ESD concept used (Zener, open base transistor (OBT) or silicon controlled rectifier (SCR)). They are limited to small currents.

Depending on the product, the applied current used to model the diode I/V characteristics is usually limited to between 20mA and 200mA. With this limitation the device does not usually trigger. For standard applications, such as USB 3.1, this limitation is sufficient and helps to avoid convergence problems in the SI analysis.

This set-up leads to a modelled leakage current, and the starting conduction is modelled as shown in Figure 1.

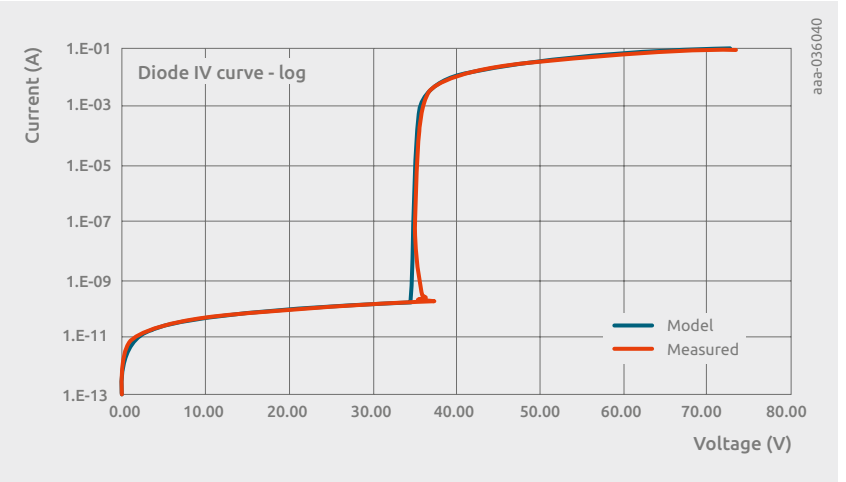

Figure 1 | Modeled and measured positive I/V curve of a DUT

The main focus of the model is the RF behavior. The product is modelled along the measured S-parameter to achieve matching behavior. Focal points are the –3 dB point of the transmission and their resonances.

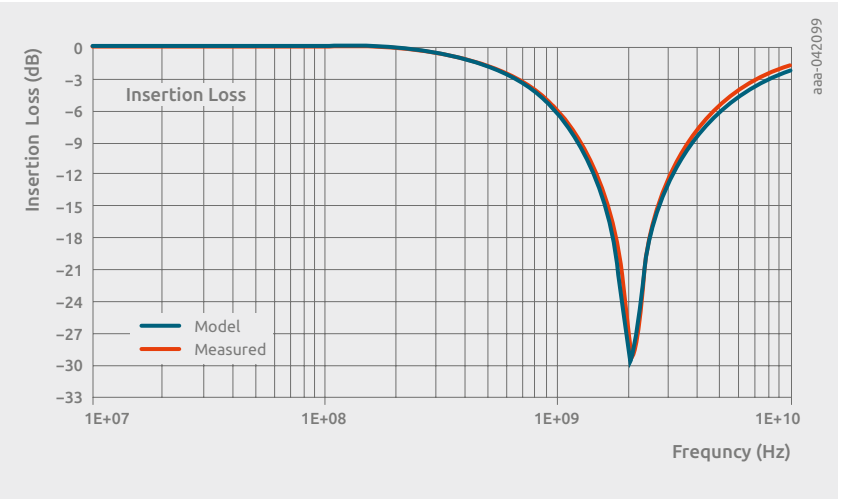

Figure 2 | Modeled and measured insertion loss of a DUT

The reflection is also modelled, as shown in Figure 3. A good model aligns closely with the measurements. For low capacitance values, more than one resonance can be seen in a typical frequency range up to 40GHz. The goal for SPICE models is to provide a fair correlation up to the second resonance.

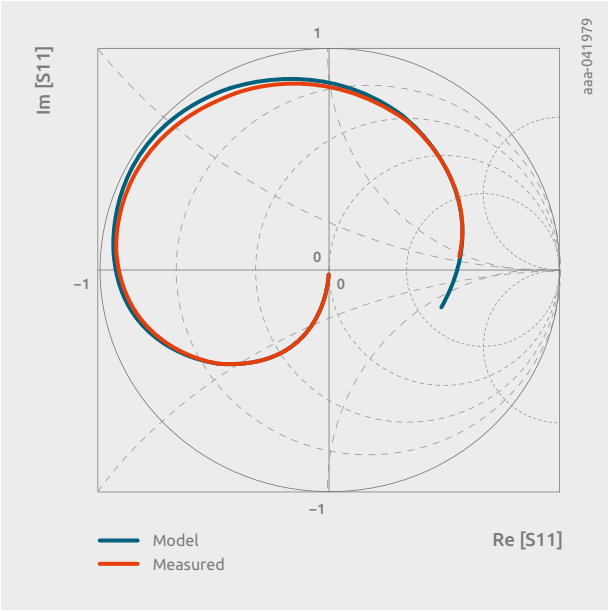

Figure 3 | Modeled and measured return loss

For multi-pin devices the crosstalk behavior is also part of the model. An example is shown in Figure 4. A good crosstalk match at least gives the maximum crosstalk at the corresponding frequency.

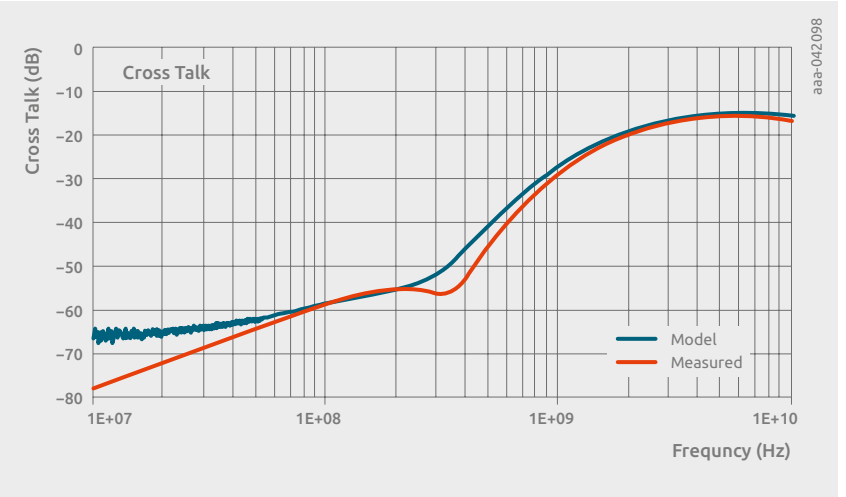

Figure 4 | Modeled and measured crosstalk of a DUT

The capacitive behavior over the measured frequency range is also modelled. Here, the model is focused on low-frequency capacitance, calculated from the S-parameter. The first resonances of the model should fit to measured data as seen in the example in Figure 5.

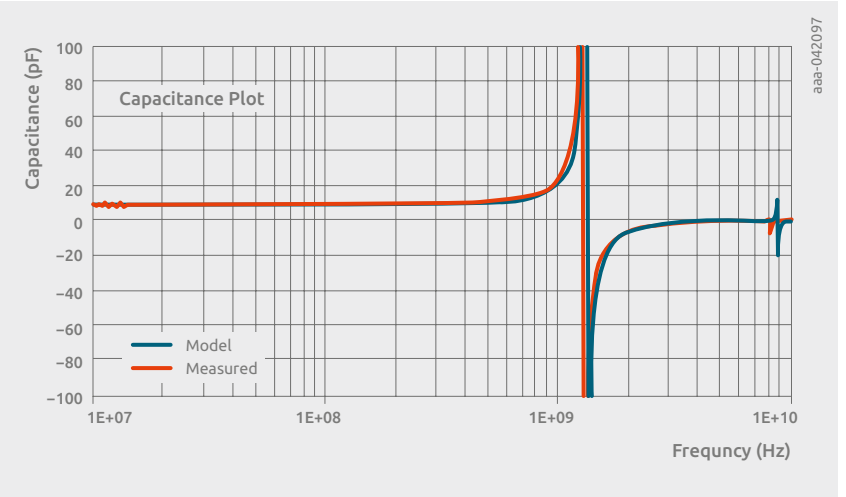

Figure 5 | Modeled and measured capacitance of a DUT

Our small signal SPICE models follow the Berkeley SPICE syntax to offer the best compatibility with most circuit simulation tools and are stored in files with the extension *.cir. These are pure text files that can be opened using any text reader. The models are valid for 25°C and are being continually improved.

The small signal SPICE models are usually not available for our PTVS (power TVS) product portfolio.

Equivalent circuits for protection devices and SoCs

Equivalent circuits for protection devices

In general, the SPICE model is divided into two parts: level one models the influence of the package and level two models the semiconductor behavior.

a) Package

The top level can be seen in Figure 6. It consists of a sub-circuit element containing the elements in the silicon die; all other elements model the RF behavior of the package and have direct physical equivalents.

Starting at each pin, there are inductances and their related resistances which are linked to the bond wires, solder pads, or conductive die attach and lead frame paths. For multi-pin packages, coupling between the pins is modelled using inductive coupling, which usually occurs mainly between the bond wires. Additional capacitive coupling between the pins is also modelled, including a resistance to cover the related quality factor of the coupling. The syntax of a typical SPICE netlist is shown in Figure 7.

```
.subckt PESD2CANFD36LQC_Q P1 P2 P3

L1 P1 _net4 650p
R_pin_t _net4 _net1 0.2
R_extra _net1 _net5 2220
C_coupl _net5 _net13 0.2
R_pin_t1 _net9 _net13 0.2
L2 P2 _net9 650p
L3 _net11 _net0 P3 0.4

X1 _net1 _net11 PESD2CANFD36LQC_Q_OB_Subdiode_cd
X2 _net13 _net11 PESD2CANFD36LQC_Q_OB_Subdiode_cd
K1 L1 L2 0.25

.ends PESD2CANFD36LQC_Q
```

Figure 7 | Syntax of a 3-pin Package with ESD protection die

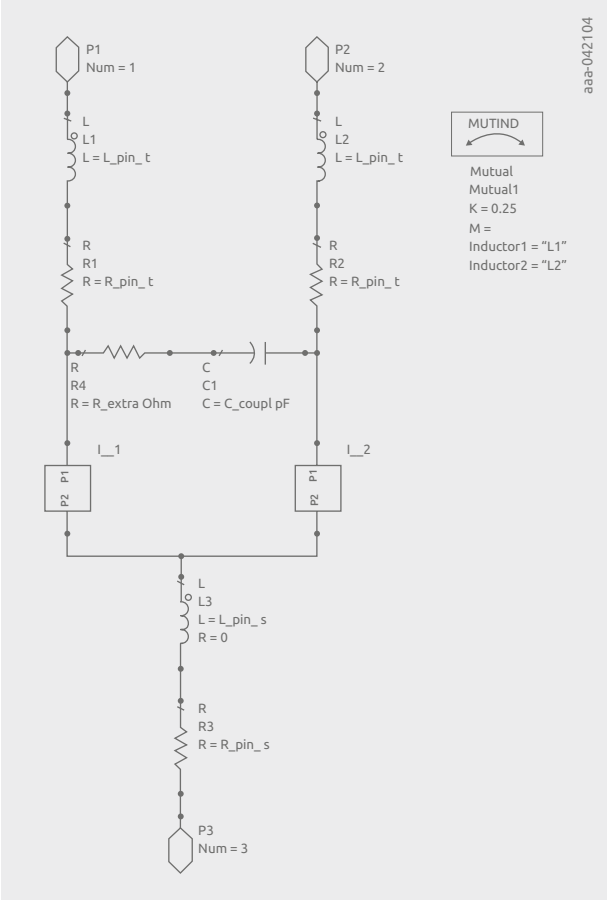

Figure 6 | Equivalent Circuit of a 3-pin Package

b) Die

The model of the die is focused on two different behaviors: the small signal DC behavior, which is usually modelled with simple bipolar elements liked diodes and/or transistors (diodes 1–4 in Figure 8), and a resistor to model the leakage current (R_LK in Figure 8).

The main influence on RF behavior is given by the junction capacitance which is placed in the model as additional capacitor (C_D_add in Figure 8). In this case C_D_add represents the capacitance of all present junctions. There are often frequency-dependent losses in the ESD protection elements that can be modelled by an RC combination in parallel to the junction capacitance. The effect of the RC combination of R_abs and C_abs is described as dielectric absorption. The schematic in Figure 8 can be easily translated to the SPICE netlist shown in Figure 9.

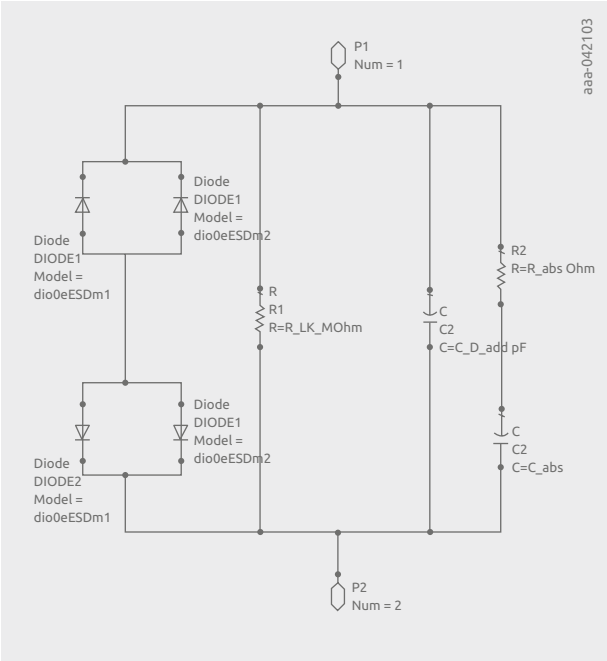

Figure 8 | Equivalent circuit of an ESD die

```
.subckt PESD2CANFD36LQC_Q_OB_Subdiode_cd P1 P2 P3

*Models
.model diodeESDm1 D Is=2.88e-16 Cjo=0.001p Bv=36.5 Ibv=1e-56u
.model diodeESDm2 D Is=3.07e-16 Cjo=0.001p Bv=63.0037
Ibv=0.06100000000039u

DIODE1 _net6 P1 diodeESDm1
DIODE2 _net6 P2 diodeESDm1
DIODE4 _net6 P2 diodeESDm2
DIODE3 _net6 P1 diodeESDm2

R_LK P1 P2 60000Meg
C_D_add P1 P2 8.3p
C_abs _net3 P2 0.2575
R_abs P1 _net3 4706

.ends PESD2CANFD36LQC_Q_OB_Subdiode_cd
```

Figure 9 | Syntax of an ESD die circuit

9.2 System Efficient ESD Design (SEED)

One of the main challenges for designers and manufacturers of electronic systems is how to combine broad application functionality that meets customer needs with sustainability in terms of electrostatic discharge (ESD) events. When ESD events occur in the field they can lead to system failures that result in short-term system upsets ('soft' failures), or even provoke physical degradation of system chip (SoC or IC) functionality leading to so called 'hard' failures.

The System Efficient ESD Design (SEED) approach helps engineers to model such electronic systems and simulate their behavior under ESD conditions. It allows designers to perform transient system-level analysis at simulation level, considering all relevant system parts in an interaction: IC, PCB, trace parasitics and SMDs as well as external ESD protection devices, providing system response on the first and second peaks of an IEC 6100-4-2 pulse [12]. Using virtual prototyping, different ESD protection concepts can be evaluated by simulation during the development phase, helping to derive the optimal ESD protection solution for a target system. Such an approach helps to minimize long development cycles, making it possible to reduce expenses and time to market for both new ESD protection components and new system designs [2–6].

Figure 10 shows an example of a system board for a USB 3.0 application which can be optimized using the SEED approach. Typically, a situation is observed in which the IC can only withstand a human body model (HBM) pulse of up to 2kV, which is only sufficient to survive through the fabrication process. When exposed to an ESD event of an IEC-like pulse, an external ESD protection device is required to extend the initial ESD robustness of the IC chip and maximize overall system ESD robustness. Instead of a trial and error approach of soldering and testing different devices on a PCB, the SEED simulation approach can be used to pre-select the optimal ESD protection solution by running a transient analysis of the given system.

A range of systems are used in different areas like mobile, automotive, computing and consumer electronics. The next section will give a general overview of the models used for configuration of the type of complex system model required for SEED simulations.

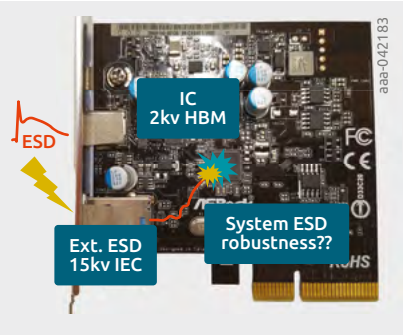

Figure 10 | System example for USB 3.0 application analysed using SEED

9.2.1 System model configuration and model types

Figure 11 shows a possible system model configuration and gives an overview of the model types that can be applied to realize each of the system model blocks.

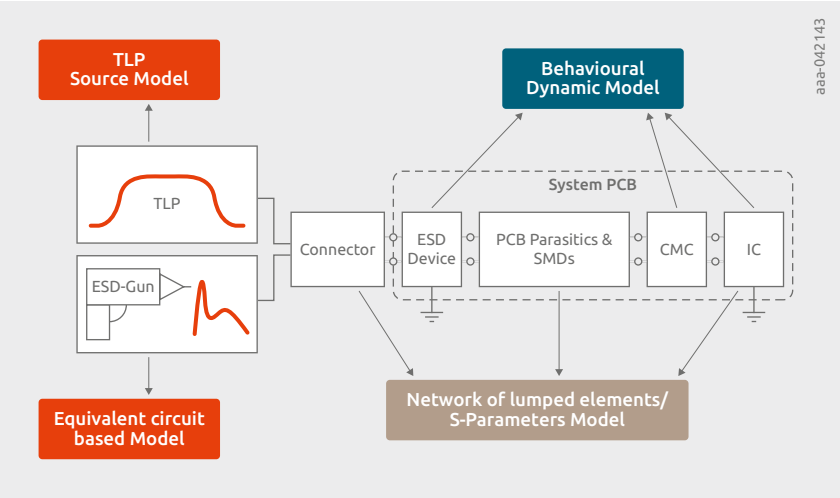

Figure 11 | System model configuration for SEED simulation

The IC, which must be protected against ESD, is located at the right-hand end of the above diagram. Its internal protection behavior can be modelled using either simple circuitry of the diode plus lumped elements (resistance and inductance), or in the case of more complex snap-back behavior by using a behavioural dynamic model approach. (This is discussed in Section 9.4.5.3.)

The second block from the right represents a model of the common mode choke (CMC). A CMC without a ferrite core is typically used for high-speed applications like USB 3.0, while CMCs with a ferrite core can be found in PCBs for automotive applications like Ethernet or CAN. CMCs with a ferrite core show strongly non-linear characteristic and are used in single-ended excitation mode (resembling the case when an ESD event is applied to one of the signal lines [14]). Such CMCs require dedicated dynamic model, which is discussed in Section 9.2.6.

The third block from the right summarizes all PCB parasitics (resistive and inductive characteristics of the traces) and SMDs (additional resistances, inductances and capacitances). These characteristics can be modelled by either a network of lumped elements or by S-parameters. Some simulators allow the user to define transmission line parameters to represent trace complex impedance.

The fourth block from the right shows the most challenging part – the external ESD protection device. To achieve optimal clamping performance and to improve the ESD robustness of a given system, snap-back types of ESD protection devices are widely used in modern circuitries. To model the strongly non-linear behavior during turn-on associated with the snap-back, a special type of dynamic model known as a switch-based behavioral model can be applied. A detailed discussion of the effects and parameters is given in Section 9.2.5.

The final, fifth block from the right represents the connector which can be modelled using a transmission-line model or S-parameter model.

When running a complex simulation like this, two different types of pulse sources can be applied: a transmission line pulse (TLP), which can be modelled using a TLP source model (whose circuitry is discussed in Section 9.2.8), or a IEC61000-4-2 pulse produced by an ESD generator, which can be modelled using equivalent circuit-based model (this is discussed in Section 9.2.7).

The much better reproducibility and defined 50 Ω environment of the TLP measurement approach compared to an ESD generator (which strongly depends on test environment conditions and user skills), together with its wide use across industry for characterization of components and circuitries, means that the TLP method can be used for characterization of all the system blocks mentioned above. Practical experience suggests TLP is also suited for system-level excitation during simulation and verification processes. The resulting level of applied TLP current into the system (TLP voltage divided by 50 Ω) can be translated into a corresponding kV failure level for ESD generator: 2 A/kV for the 2nd IEC peak and 3.75 A/kV for the 1st IEC peak. (For further details see [15].)

9.2.2 Software and simulation tools overview

Various software tools and description languages that enable system-level simulation are established across industry. Figure 12 shows some of the most popular.

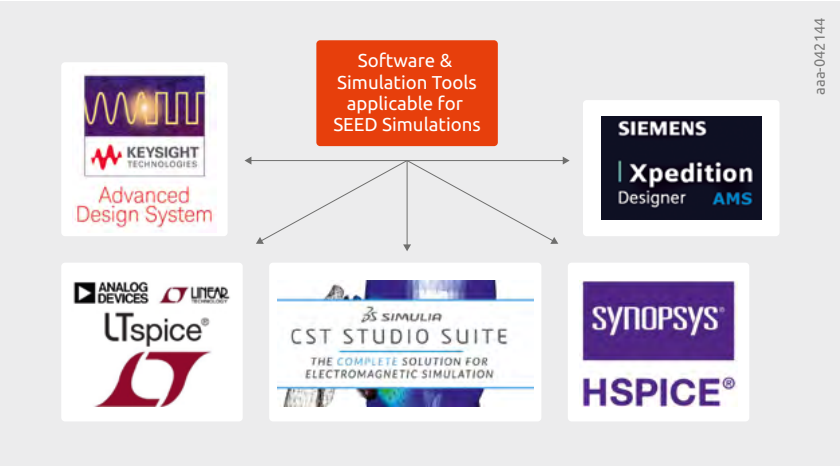

Figure 12 | Simulation software tools applicable for transient system-level SEED simulations, giving opportunities to create/use models in SPICE, VerilogA and combine 3D full-wave and 2D circuitry transient simulations.

Standard SPICE-based software tools from various companies are widely used across industry for transient system-level SEED simulations; examples include ADS from Keysight and LTSpice from ADI. Alternative software which also allows the user to implement logic using the VerilogA hardware description language is provided by Xpedition AMS from Siemens. In addition, HSPICE-based software from Synopsys is often the tool of choice for companies dealing with ICs and SoCs. CST from Dassault SIMULIA makes it possible to perform co-simulation of 3D structures including PCB and components, together with 2D circuitries, eventually combining both the full wave and the transient simulation modes.

9.2.3 System IC failure scenarios during ESD events

During ESD events, the external ESD protection device should be able to protect the whole system. That includes not only system IC, but also sensitive passive components placed on the signal trace. To achieve this, the protection device used should be placed as close as possible to the connector and have two properties. It should turn on very quickly to achieve minimal voltage overshoot associated with conductivity modulation, and have as low on-resistance (also marked as dynamic

resistance) as possible. Also, its parasitic inductance (due to wire bonds and metallization contacts) should be low so that it makes a minimal contribution to the voltage overshoot produced during the turn-on process. The parameters of the ESD protection device, together with the signal trace and SMDs characteristics and the IC internal ESD protection parameters, define the ESD robustness of the whole system.

We will now discuss two different failure scenarios for the IC.

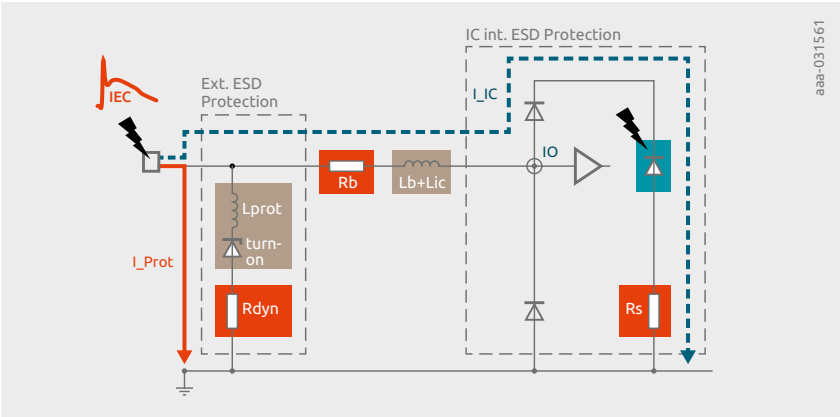

Figure 13 | A simplified example of the equivalent circuit of a system, consisting of external ESD protection component, signal trace parasitics and rail-to-rail internal ESD protection of the IC. The system dynamic and quasi-static parameters are marked with brown and orange frames, respectively.

The first scenario describes the situation where the sensitive gate oxides of MOSFET transistors are destroyed by voltage overshoot during the first couple of nanoseconds of an ESD pulse. In automotive applications, this kind of failure is more likely in the multimedia and high-speed SerDes interfaces than in classic In-vehicle networks (IVNs).

Figure 14 shows an example where the dynamic voltage overshoot, which occurs at the I/O pin, exceeds the limit of the IC's maximum permitted voltage drop. The red curve shows the corresponding voltage drop across the external ESD protection device.

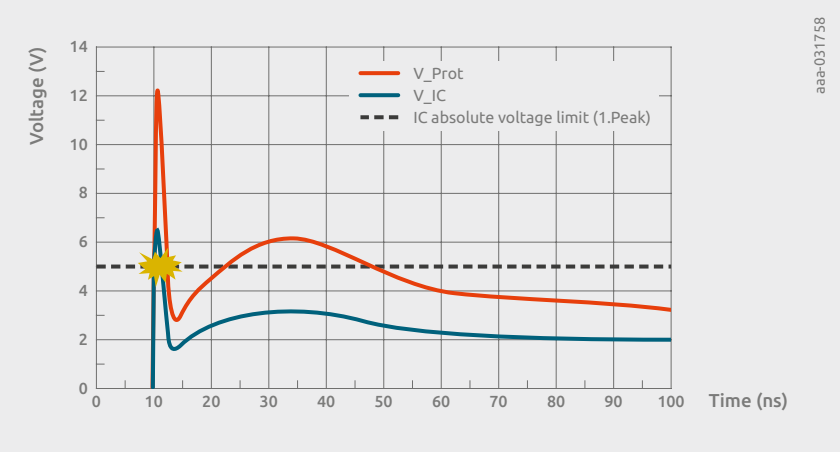

Figure 14 | Evaluation of voltage in time domain. The blue curve shows the voltage overshoot at the IC internal I/O pin, the red curve indicates the voltage drop across the external ESD protection device, the dashed black line defines the absolute IC voltage limit.

Two factors can influence the distribution of dynamic overshoot further into the system. The first is the turn-on behaviour of the external ESD protection device, also known as conductivity modulation [7] and its parasitic inductance. The second is the ratio of parasitic inductances in the system, forming a voltage divider $V_{prot} / (V_{trace} + V_{ic})$. Proper modelling of device or system reaction to the rising edge of the ESD pulse is therefore essential for correct representation of dynamic system-level behavior. While inductive behavior can be relatively easily modelled by adding lumped elements to the simulation, a significant challenge emerges of how to model the turn-on behavior of the external ESD protection device, especially if it is a protection device with snap-back.

In the second scenario the system is subject to high power dissipation inside the IC due to the high current flow through the IC's internal ESD protection. This leads to thermal system damage referred to as electrical overstress (EOS). In this situation the ratio of the system resistances $R_{prot} / (R_b + R_s)$ defines the amount of residual current that flows into the IC. Figure 15 shows the residual current inside the IC's internal ESD protection (blue curve) together with the current of the external ESD protection device (red curve).

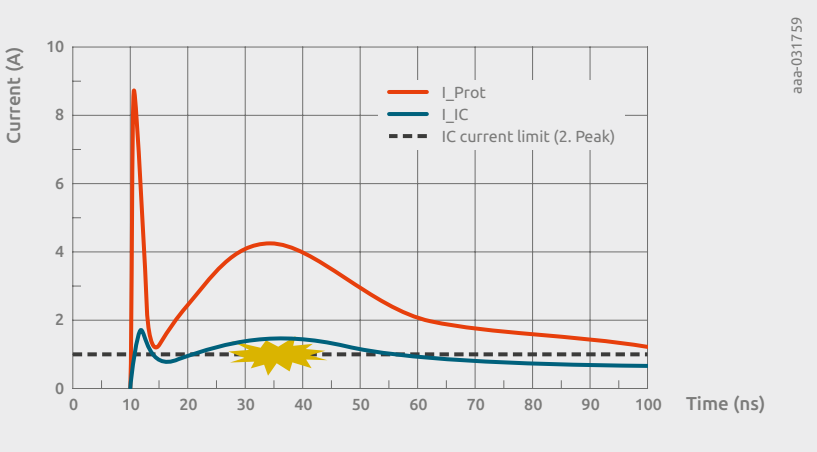

Figure 15 | Evaluation of current in time domain. The blue curve shows the residual current through the IC internal ESD protection, the red curve indicates the current through external ESD protection device, the dashed black line defines the IC current limit in steady state condition.

9.2.4 IC ESD safe operating area determined by TLP

To characterize the whole system in terms of system-level ESD robustness the safe operating areas (SOA) of the protected IC should be identified first for both of the failure scenarios that have been described.

The IV and IV_{max} data needed to describe the quasi-static and dynamic behaviour of the device under test (DUT) can be acquired using the TLP measurement method [9]. Figure 16 shows schematically how the current and voltage characteristic of the device in time domain, obtained by variation of applied pulse amplitude and constant rise time, can be captured.

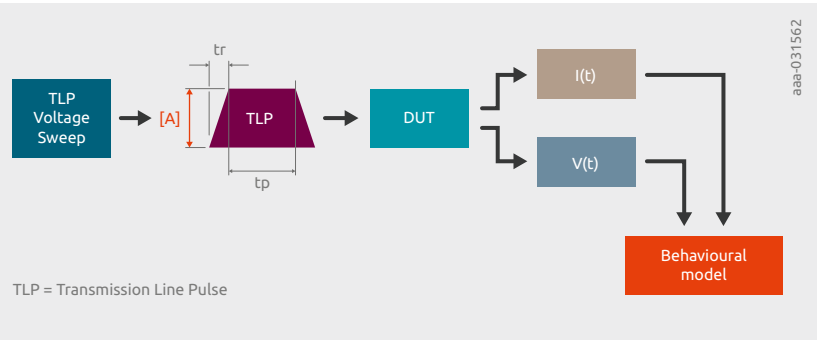

Figure 16 | Principle of acquisition of time domain IV and IV_{max} characteristic of the DUT using

transmission line pulse measurement to tune behavioral models of IC internal ESD protection devices and external ESD protection components.

For quasi-static behavior, all averaged values of current and voltage time-domain curves evaluated in the time window of 70 ns to 90 ns are combined to describe the IV characteristic of the DUT. To describe the dynamic characteristic, the first couple of nanoseconds for both current and voltage are evaluated to calculate voltage overshoot vs. current (IV_{max}). The extracted IV and IV_{max} curves can then be used as the basis for tuning of quasi-static and dynamic behavioural models applicable for both external and IC internal ESD protection circuitries.

Eventually, the SOA of the IC can be derived from IV data measured by TLP. Figure 17 shows an example of IV curve where the quasi-static failure level was detected by measurement of leakage current through the internal ESD protection device of the IC after each applied pulse. Subtracting 20% from the failure current provides a substantial safety margin for a given IC. The same approach can be applied to obtain the IV_{max} characteristic of the DUT.

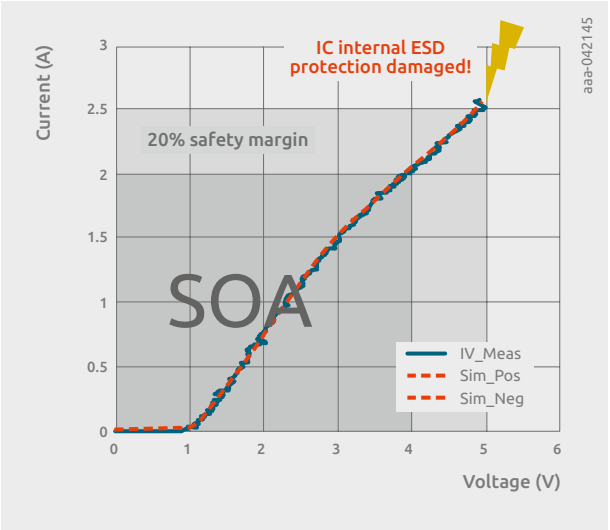

Figure 17 | Definition of safe operating area (SOA) of an IC's internal ESD protection using IV data obtained from transmission line pulse (TLP) measurement method to identify system-level ESD robustness. For this standalone IC, 1 kV IEC ESD robustness can be expected. To extend this level, all relevant system parts as described in Section 9.2.1 need to be considered in a system-level SEED simulation.

9.2.5 Modelling of ESD protection devices with snap-back

Modelling snap-back behavior requires a more sophisticated approach than the standard Berkeley SPICE model, which although it allows the small-signal behavior of diodes to be represented can only be extended in limited ways to high current, as shown in Figure 18.

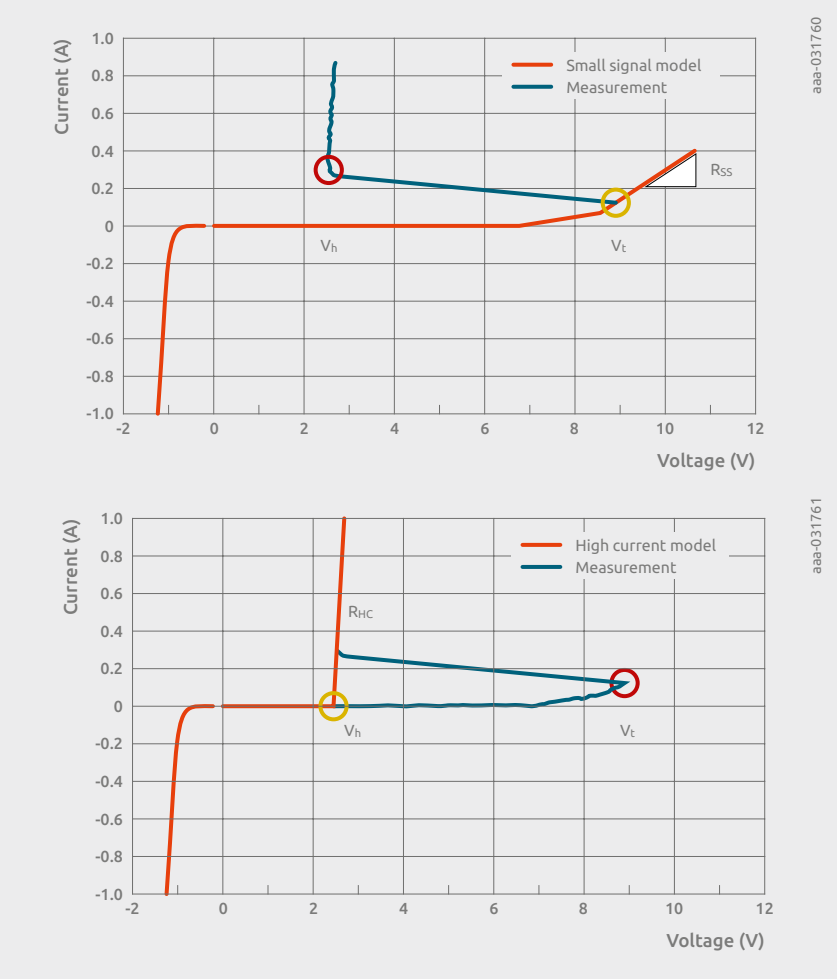

Figure 18 | The top graphic shows the small-signal modelling results of an external ESD protection device with snap-back; the graphic at the bottom illustrates the high current model.

For precise transient analysis of a system from the perspective of both failure scenarios discussed earlier in this chapter, the SEED model of ESD protection device should be applied to both quasi-static and dynamic behaviour. Special attention should be given to modelling of snap-back, including all related dynamic effects, to describe the non-linear behaviour during device turn-on on the one hand, and the self-heating effect at higher currents on the other.

Dynamic SEED model tuning by TLP

The main aim of the fully dynamic SEED approach is to combine all effects into one model. Figure 19 illustrates all the relevant regions that need to be modelled for a snap-back type of ESD protection device: small-signal, snap-back (non-linear), high-current (linear) and self-heating (non-linear).

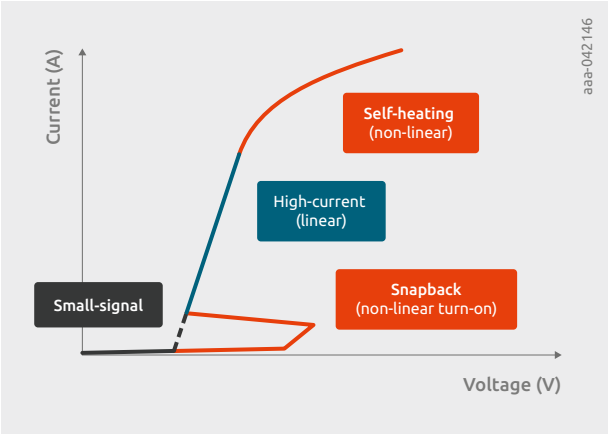

Figure 19 | All relevant regions of a snap-back type of ESD protection device: small-signal, snapback (non-linear), high-current (linear) and self-heating (non-linear).

To capture the quasi-static and dynamic behavior, TLP time-domain curves are evaluated as described in Section 9.2.4. Figure 20 shows the example of an IV curve constructed point by point (left) from corresponding TLP data and the corresponding working regions to be included into simulation for quasi-static IV behavior (right).

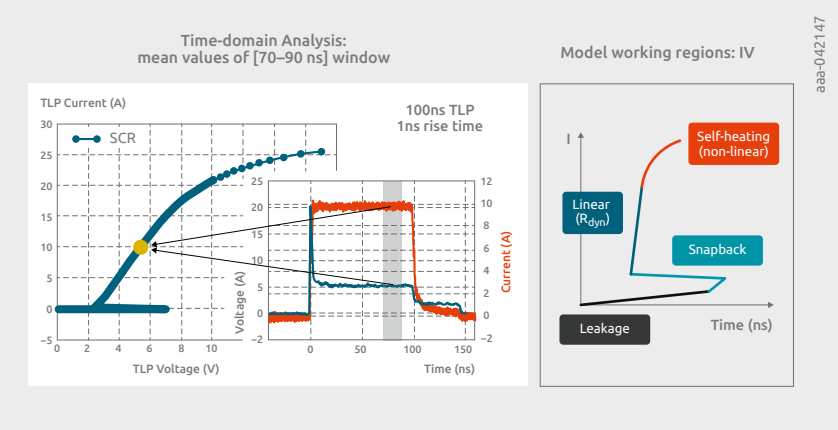

Figure 20 | Dynamic model tuning by TLP. Quasi-static behavior of an ESD protection device with snap-back showing construction of IV curve (left) and model working regions (right).

To capture the dynamic behavior, either TLP or Very Fast TLP (VF-TLP) can be applied. In the case of VF-TLP the applied pulse duration is reduced from 100ns to 5ns. This allows the impact of high-power dissipation within the DUT to be excluded, preventing self-heating and giving more focus to turn-on behaviour.

Figure 21 shows an example of an IV_{max} curve constructed point by point (left) from corresponding TLP data and the corresponding regions to be included in the simulation (right).

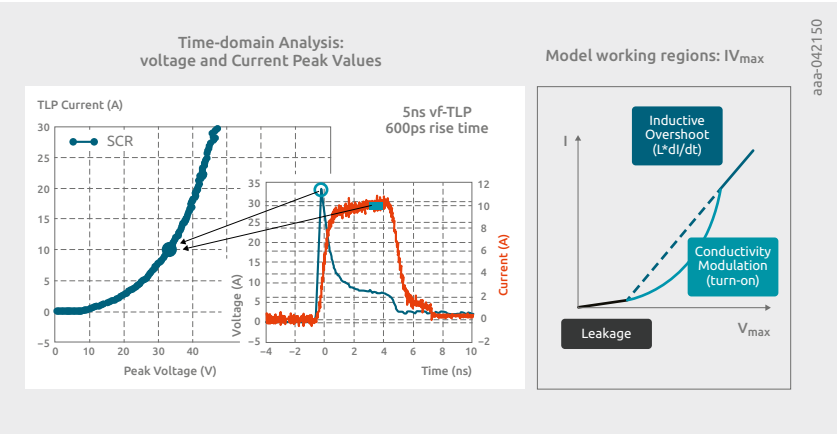

Figure 21 | Dynamic model tuning by TLP. Dynamic behavior of an ESD protection device with snap-back showing construction of IV_{max} curve (left) and model working regions (right).

Dynamic SEED model parameters

To tune the model, different model parameters and effects need to be considered. Figure 22 shows all relevant parameters that need to be incorporated in a dynamic SEED model.

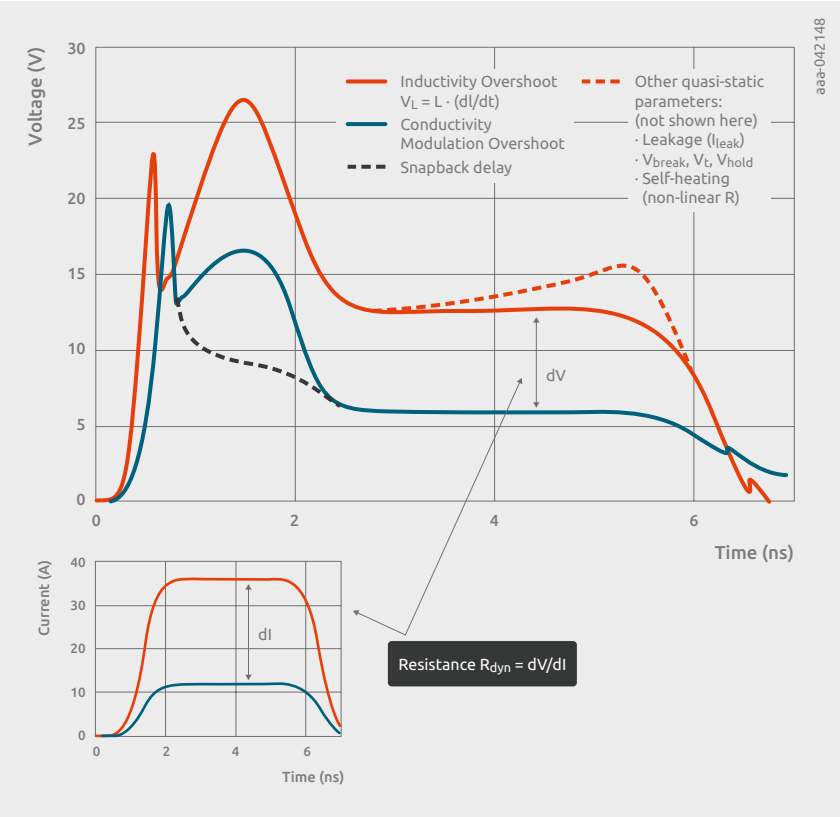

Figure 22 | Dynamic model parameters overview.

To model dynamic behaviour of a device with snap-back and properly reflect its dynamic overshoots, several effects need to be considered: conductivity modulation overshoot, inductive overshot and snap-back delay.

For quasi-static behaviour, the main parameters are leakage current, breakdown voltage, trigger voltage, holding voltage, dynamic resistance and self-heating resistance.

All these effects and parameters can be tuned based on time-domain current and voltage curves as well as on corresponding IV and IV_{max} curves obtained from TLP.

Implementing a switch-based dynamic SEED model in ADS

The goal of behavioral dynamic models is to extend quasi-static models with dynamic characteristics of the given ESD protection device to be able to carry out full system-level transient analysis for SEED. This means that component reaction to the injected ESD pulse needs to be analysed during two different time frames: the first reflects the impact of current to time ratio (dI/dt) of the rising edge of an injected ESD pulse on device behavior during the first couple of nanoseconds. The second is related to its steady state condition, reflecting the window between 70 ns and 90 ns. We will now discuss the relevant working regimes and effects, as well as the approach to implement the dynamic model for an ESD protection device with snap-back.

First, quasi-static behaviour will be considered. Figure 23 shows the typical IV curve of an ESD protection device with snap-back and had four related working regions.

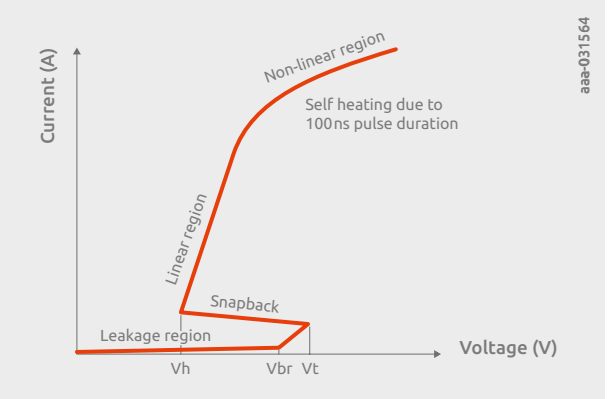

Figure 23 | The quasi-static IV curve of an ESD protection device with snap-back with four working regions: leakage, snap-back, linear and non-linear.

The first region is the leakage region. Here, device behaviour can be approximated by small-signal device characteristics using SPICE based models. However, since the signal integrity is not within the scope of the transient ESD analysis, simple approximation of leakage current by considering resistance and breakdown voltage V_{br} should be sufficient. The second region is the snap-back region. Here, the triggering voltage point is defined by V_t, at which the snap-back to holding voltage V_h occurs. The third region is the linear region. This regime is defined by a constant resistance value. The fourth region is the non-linear region. Due to self-heating of the device a bending of the IV curve can be observed. To express this behavior additional resistance will be added. The quasi-static IV curve, which is needed for model tuning, is obtained by TLP. In that case, averaged values of voltage and current in the window from 70 ns to 90 ns time are used.

Figure 24 shows an example of the implementation of the dynamic model in ADS, adapted from [6].

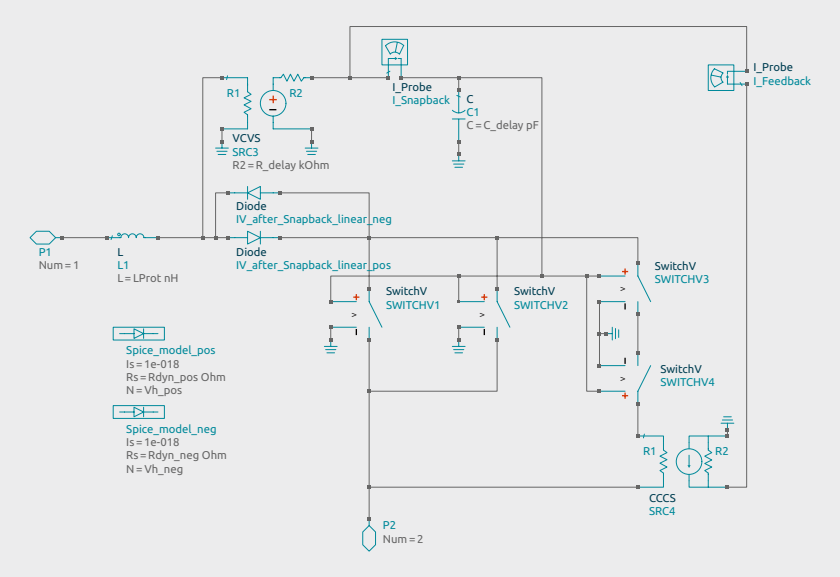

Figure 24 | Dynamic model circuitry of an ESD protection device with snap-back implemented in ADS for SEED including full quasi-static and dynamic working regimes without snap-back delay.

In this model, both the leakage region and the linear region of the device are defined by SPICE model parameters. The snap-back and non-linear regions are implemented with the help of voltage-controlled switches. Each switch represents a change in resistance dependent on voltage. The voltage-controlled voltage source (VCVS) together with resistor and capacitor belong to a control unit that is used to control the switches. A current feedback loop, which is realized using a current-controlled current source (CCCS), is an essential part of the model for the realization of snap-back behavior, since it can keep all switches in pre-defined positions by feeding the current back into the control unit even after the triggering voltage point of the device is reached and the VCVS is no longer able to transfer the initial voltage level to the capacitor of the control unit.

Figure 25 shows an example of current flow after snap-back has occurred and the model already operates in the linear region. The green arrows in the picture indicate how the current is flowing during that time.

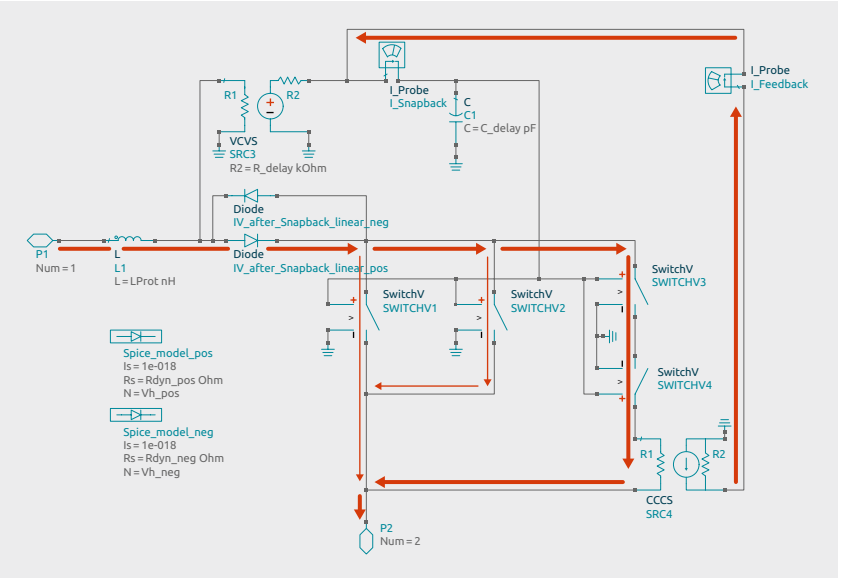

Figure 25 | Current flow in the dynamic model for ESD protection device with snap-back without snap-back delay, in the linear working regime for steady state condition.

Now, consider dynamic behaviour. Figure 26 shows a typical IV_{max} curve, generated from the maximum values of TLP measurement, of an ESD protection device with snap-back. It includes two effects which are responsible for voltage overshoot on the device: inductance (L_{Prot}) and conductivity modulation (CM) [7].

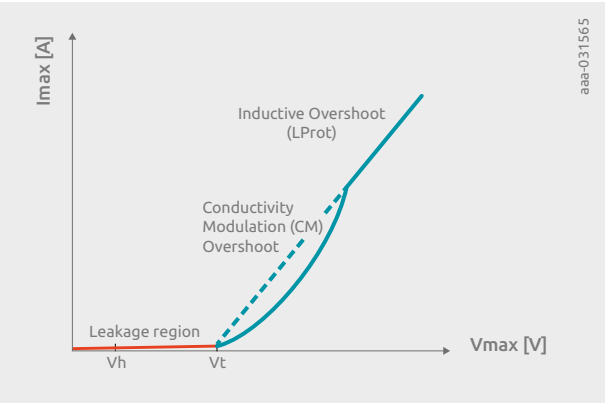

Figure 26 | The dynamic IV_{max} curve of an ESD protection device with snap-back, showing two effects: inductive overshoot (L_{Prot}) and conductivity modulation (CM) Overshoot.

The first effect is related to the parasitic inductance of the device. This can be easily implemented in the model with the help of lumped element. In this case, inductive overshoot is modelled according to L_{Prot} *dI/dt. The value for L_{Prot} can be estimated from VF-TLP data or measured using a network analyser. The value obtained for L_{Prot} is usually different from the parasitic inductance considered for signal integrity.

The second effect describes the conductivity modulation of the device, which is related to its turn-on behaviour. The impact this effect has on total voltage overshoot depends on the technology used. To model a device's resistance change during turn-on, an RC network is used (see R (parameter of VCVS) and C capacitor of the switch control unit in Figure 25). Depending on dI/dt of the injected ESD pulse and the RC value, the overshoot of the ESD protection device can be modelled.

Figure 27 shows an example of dynamic transient simulation of both inductive and CM voltage overshoots. Here, each curve represents model reaction on TLP pulse with different current amplitudes but constant rise time.

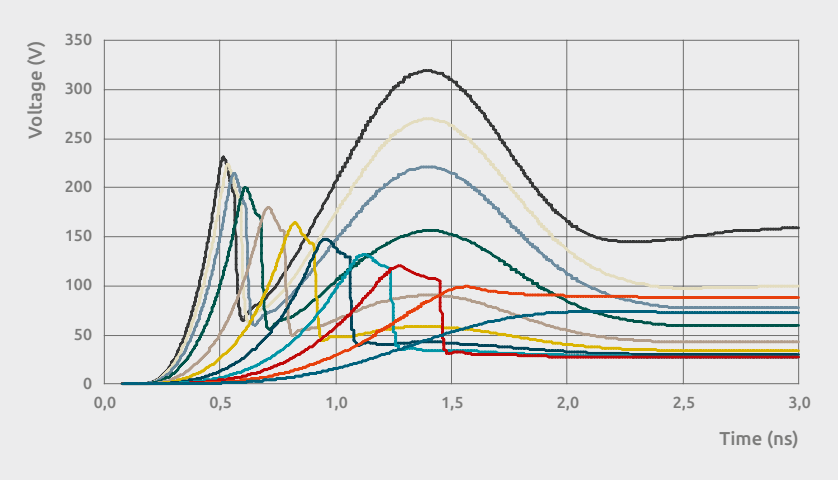

Figure 27 | The time domain curves of the inductive and conductivity modulation voltage overshoots modelled with dynamic modelling approach without snapback delay by application of TLP with different current amplitudes by constant rise time.

Although this model can replicate dynamic behaviour well, one additional effect needs to be considered that should be included in the model implementation. This is related to the delay of transition from voltage at the triggering point before snap-back to the voltage level after snap-back, according to the current level of the ESD pulse that is applied. In the model, snap-back delay prevents an abrupt decrease in voltage after the CM peak is reached. Here, current already starts to flow through the device by keeping the voltage across the device at about triggering voltage and slowly decreasing it. Only in this case can correct modelling of both CM and inductive overshoots be carried out simultaneously. Figure 28 shows the simulation result of both inductive and CM voltage overshoots after snap-back delay has been added into the model circuitry.

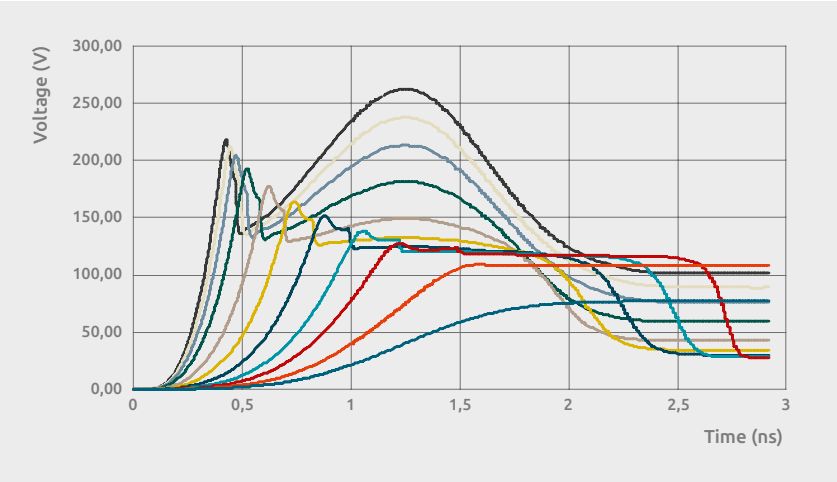

Figure 28 | Time domain curves of inductive and conductivity modulation voltage overshoots, obtained using a dynamic modelling approach with snap-back delay by application of TLP with different current amplitudes by constant rise time.

This is realized using additional CCCS with current loop and another switch, which define the charging speed of the capacitor C in the switch control unit and delay full current transition via the current feedback loop. Figure 29 shows the complete version of the model.

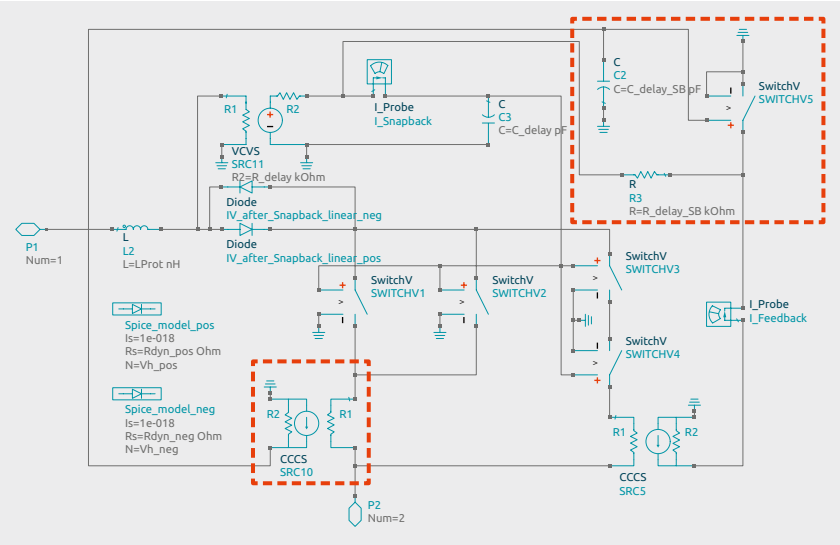

Figure 29 | The dynamic model circuitry, including snap-back delay part, of an ESD protection device with snap-back implemented in ADS for SEED including full quasi-static and dynamic working regimes.

Finally, it should be mentioned that this model can be also used bi-directionally and for both positive and negative pulse excitations, representing the behavior of a bi-directional ESD protection device with snap-back, where both directions can be tuned separately and independently using dedicated sets of variables. Figure 30 shows the complete dynamic SEED model.

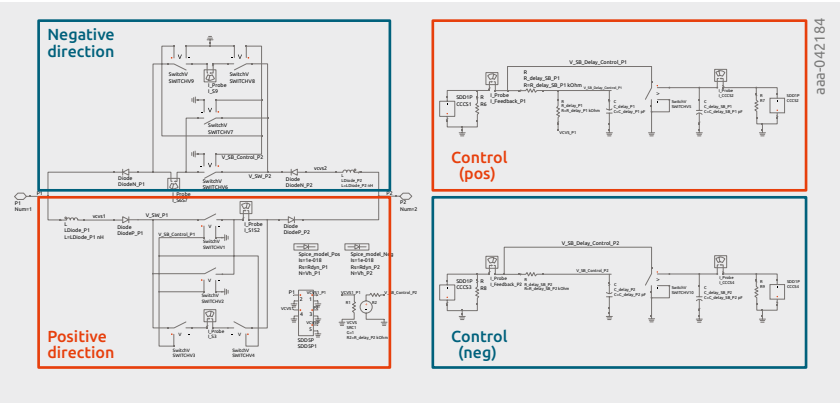

Figure 30 | The fully dynamic bi-directional and bi-polar SEED model for ESD protection device with snap-back implemented in ADS software.

9.2.6 Modelling of common mode choke for SEED

The common mode choke (CMC) is primarily used in a system to suppress the common mode noise of the entering signal. However, a sometimes-hidden advantage manifests itself in its ability to suppress ESD pulses that can impair system performance and lead to upsets or even degradation. Since use of CMC alone is typically not enough to guarantee a high level of system ESD robustness, a combination with an ESD protection device is often suggested. This symbiosis can sufficiently improve the final ESD robustness of the system.

Typically, S-parameters will be obtained to characterize and model CMC behavior. A problem arises, however, when a CMS with a ferrite core is used. In that situation, effects like saturation start to play a significant part, since the current flow can no longer be suppressed. To include this effect and capture its dynamic characteristic, reflected as current overshoot due to turn-on of the CMC, an appropriate model beyond small-signal range is needed. Figure 31 shows the results of an extended CMC model, based on the adapted dynamic modelling approach described in Section 9.2.5 and including S-parameters of the CMC.

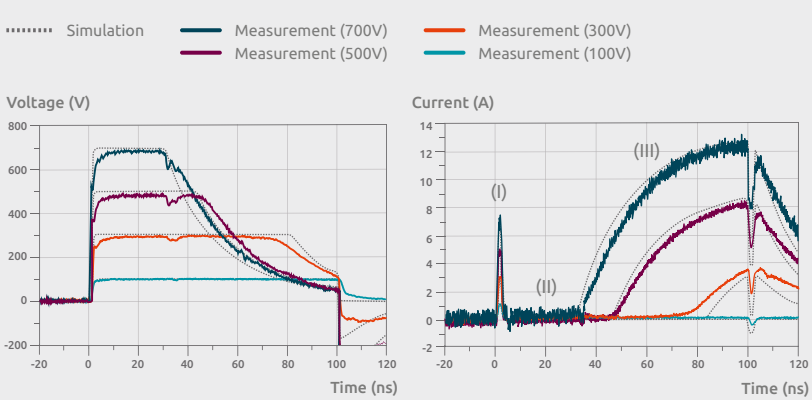

Figure 31 | Simulation results of the CMC model compared with measurements representing both dynamic (I) and quasi-static: small-signal(II) and saturation (III) working regions.

Evaluating voltage and current curves in the time domain allows two working regimes to be identified: dynamic and quasi-static. The dynamic behavior of the CMC is reflected by the rising edge of voltage and corresponding current peaks (I). Here, the CMC works as an inductor. The quasi-static behaviour of the CMC can be sub-divided into two further regions: small-signal (II), where the CMC transforms the open condition of the second coil preventing the current flow through the first coil and keeping the voltage at the constant level, and saturation region (III), a point where the energy can no longer be stored inside the CMC, which starts to change its characteristic to a resistance, whereby the current starts to flow and voltage drops dramatically. Further details about the model can be obtained from [14].

9.2.7 ESD generator model implemented in ADS

For transient analysis of modelled system behaviour during an ESD event, an ESD pulse model is required. An ESD generator is used to replicate ESD events that can occur in the field. Therefore, for accurate evaluation of system-level behavior an ESD generator model is used in SEED. Figure 32 shows an example of how the ESD generator model can be implemented in the form of an equivalent circuit. This model is based on the modelling solutions proposed and discussed for ESD generators in [8–10].

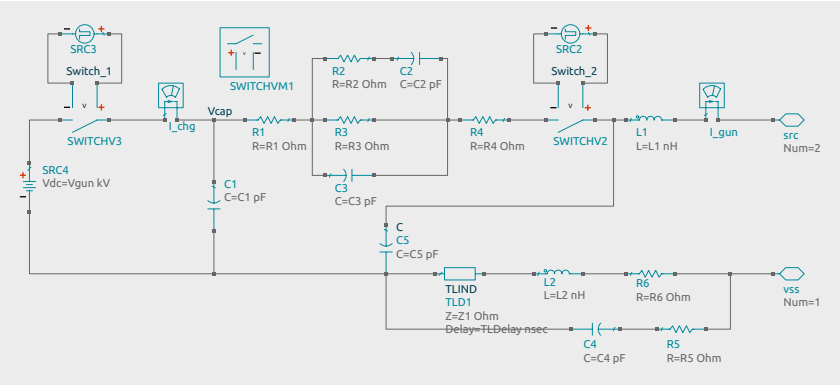

Figure 32 | Equivalent circuit-based model of ESD generator implemented in ADS

Before this model can be used as a stimulus for a system-level transient analysis it should first be tuned using the calibration measurement results of the ESD generator. Figure 33 shows the comparison of simulated and measured time domain current curves. The measured curve was obtained according to the setup defined in the IEC61000-2-4 standard, while a 1kV ESD pulse was injected into a 2 Ω Pellegrini target.

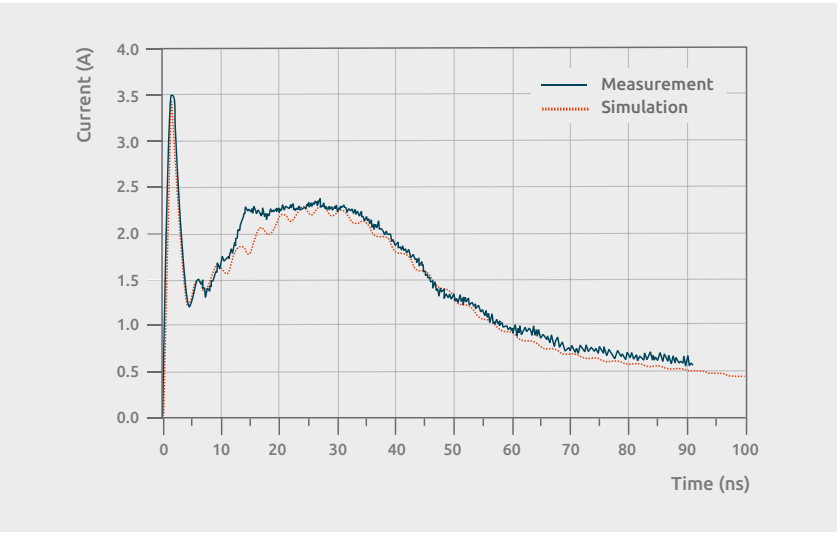

Figure 33 | Simulation result of an ESD generator model tuned on a time domain current curve obtained by calibration according to the IEC61000-4-2 standard

9.2.8 TLP Source model implemented in ADS

The TLP source model is an essential part of SEED simulation and is used for tuning of all system models as well as a stimulus for the overall system-level simulation. Figure 34 shows the circuitry in ADS for the TLP source model.

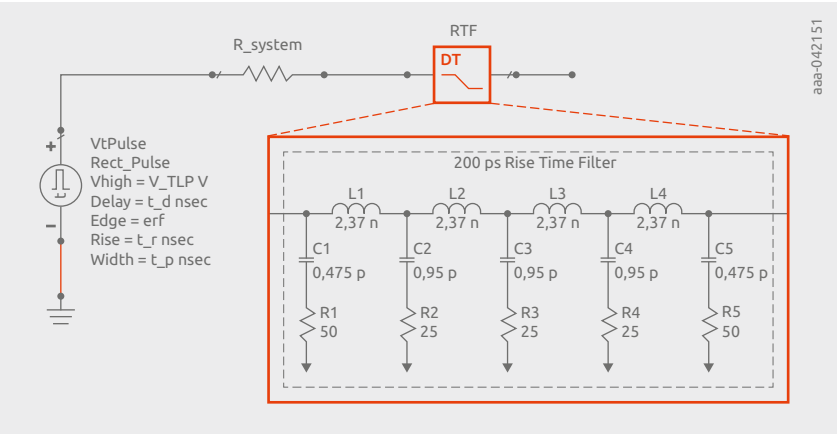

Figure 34 | TLP source model implemented in ADS, consisting of a rectangular pulse source, system resistance and rise-time filter. This can be used for behavioral model tuning of ESD protection devices, CMCs and IC internal ESD protection circuitries, and as a stimulus for system simulation.

To achieve high accuracy, the model needs to be tuned using measurement data. Figure 35 illustrates the outcome and how different parts of dynamic overshoot are related to pulse form and rise time. System resistance R_system = 50 Ω and rise-time t_r = 1ns are used. An error-function curve is used to define the edge of the pulse. To define a smooth transition between high and low voltage, a rise-time filter is added in series.

Two parts of the curve are important for proper dynamic behaviour modelling: the pulse form at low currents, which defines the conductivity modulation (CM) overshoot, and the pulse rise time (di/dt), which defines the inductive overshoot (VL=L*di/dt). Correct adjustment of the pulse amplitude via V_TLP is important for accurate modelling of quasi-static behaviour (dynamic resistance or clamping) of the DUT.

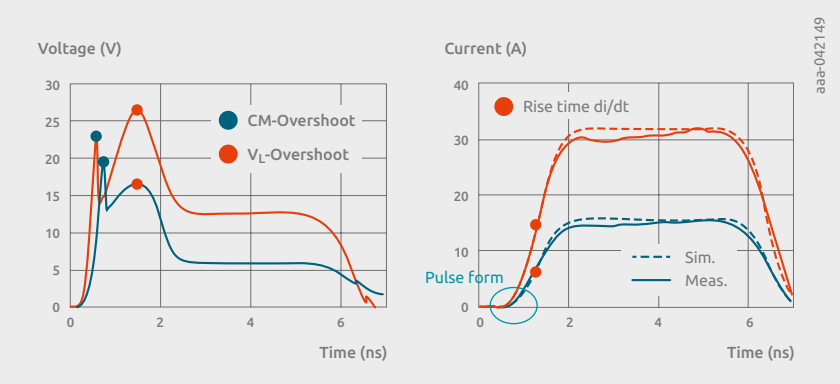

Figure 35 | The plot on the right shows a comparison between modelled and simulated time-domain current curves indicating rise time and pulse form which determine VL-overshoot and CM-overshoot, respectively, as shown on the left-hand plot.

9.2.9 Applying SEED methodology to simulate 100BASE-T1 Ethernet

The OPEN Alliance has specified an ESD protection network for 100BASE-T1 and defined test procedures to test compliance of external ESD protection devices (see Section 7.4). According to this specification the ESD protection device is placed in front of the CMC. This helps to not only trigger the ESD protection device earlier, due to CMC, but also to protect passive components located on the signal trace against ESD. Moreover, the position of the external ESD protection device eliminates the need to adapt its characteristics to IC requirements, making selection and later exchange of ESD protection components or ICs more flexible and independent of each other.

An ESD discharge current test allows the ESD robustness of the system to be predicted [1]. This test determines the rest current that flows into the system IC during an ESD event and helps to identify whether the ESD protection device used for protection of a 100BASE-T1 transceiver can guarantee a certain level of ESD robustness. For that purpose, an ESD gun test is carried out using a test board as shown in Figure 36.

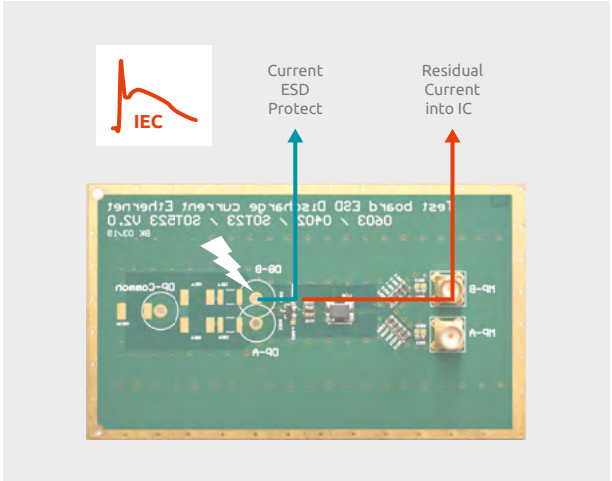

Figure 36 | The IEC pulse of an ESD generator is injected into the external pin of the test board leading to current spread between the external ESD protection device and the IC, allowing residual current flow into the IC to be evaluated.

We will now show how the SEED methodology can be applied to model this test procedure, in order to predict the current flow into the IC during an ESD event at a simulation level and to draw conclusions about the ESD robustness of the overall system including ESD protection. The treatment is a general one; for more detailed information refer to the white paper 'Efficient prediction of ESD discharge current according to OPEN Alliance 100BASE-T1 Specification using SEED' [2], which is available on the Nexperia website.

To perform a transient simulation of a 100BASE-T1 ESD protection network, each part of the system should first be modelled. Figure 37 provides an overview of the equivalent circuit block diagram of the SEED model of the ESD discharge current measurement reference circuit, according to the OPEN Alliance Specification, for the PCB shown in Figure 27.

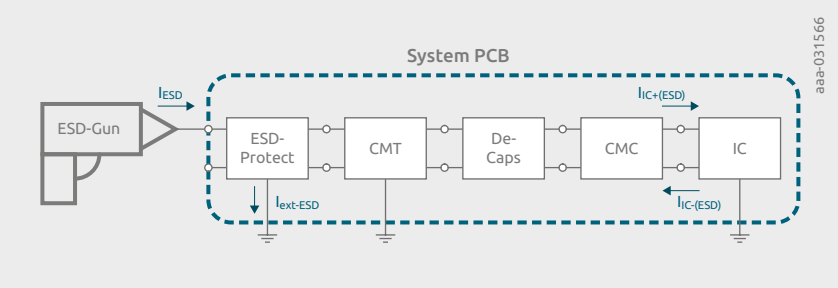

Figure 37 | Equivalent circuit block diagram for the SEED model of the ESD discharge current measurement reference circuit according to the OPEN Alliance specification [1].

Each of the blocks depicted here represents a model optimized for SEED. All the models can be grouped into three types: equivalent circuit-based models (ESD gun), models that can be implemented in the form of networks with lumped elements (common mode termination (CMT), de-caps and IC) and behavioral model (ESD protection device, common mode choke (CMC)).

A PESD2ETH1G-T component was chosen to protect the system against ESD. One of the challenges here was to ensure that the ESD protection device triggers before the CMC goes into saturation mode, where the current flow into the IC rapidly increases and may damage the system. To ensure that this happens, a safety margin of about 50 % between the triggering point of the ESD component and onset of saturation was achieved by choosing an appropriate combination of ESD protection and CMC components. Figure 38 visualizes the CMC I-V curve including the triggering point V_t_ext_ESD of the ESD protection device used in this example.

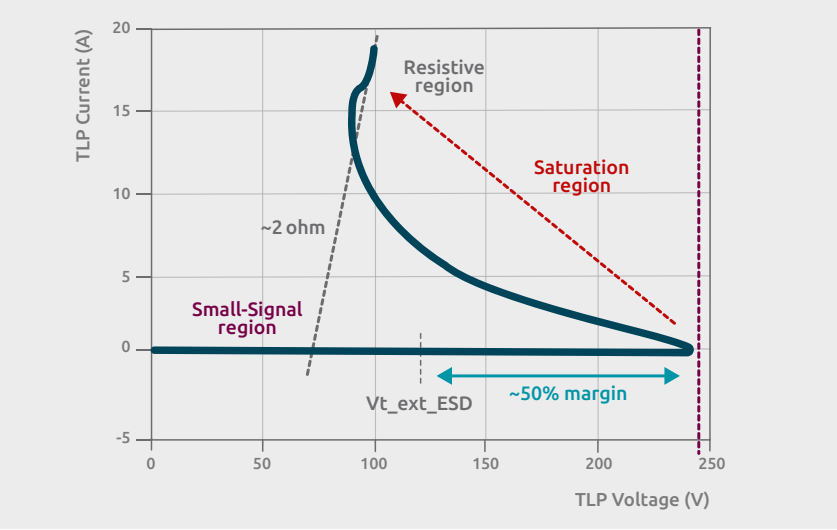

Figure 38 | The I-V curve of the CMC obtained by TLP shows small-signal, saturation and resistive working regions. The V_t_ext_ESD voltage triggering point of the external ESD protection device indicates a safety margin of around 50% to the onset point of saturation of the CMC component.

The corresponding simulation results of quasi-static and dynamic behavior of a PESD2ETH1G-T ESD protection device, whose dynamic model is discussed earlier in this chapter and is depicted in Figure 30, can be observed in Figure 39.

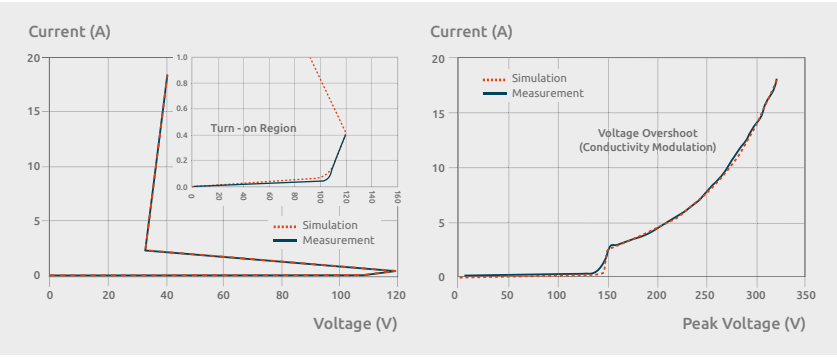

Figure 39 | The top graphic shows the simulation result of the quasi-static I-V curve of the PESD2ETH1G-T ESD protection device including a detailed zoom-in on its turn-on region. The bottom graphic shows an overview of its dynamic characteristic, described with a I-Vmax curve.

Finally, the residual current flow into the IC is evaluated, using the full SEED model depicted in Figure 30. In Figure 40 the comparison of simulated versus measured rest current flow into the IC is shown. Here, a positive ESD generator discharge of 4 kV into the external system pin is applied and evaluated.

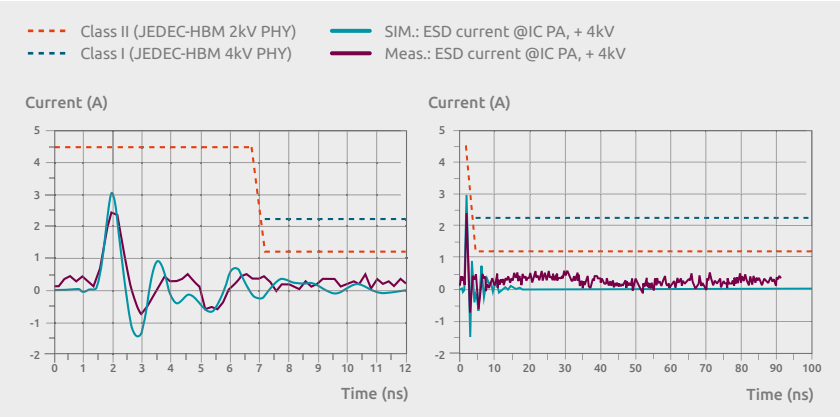

Figure 40 | Time domain curves of measured v. simulated residual current into the IC with focus on dynamic (left) and quasi-static (right) behaviour.

Both graphics include the simulated current curves in time domain concurrently, showing the measured current at the IC I/O pin. The yellow and red dashed lines show the limits of Classes I and II of the JEDEC-HBM standard [11], respectively. The SEED model used here provides an estimate of the tested system and predicts a maximum current peak that is around 20% higherk. For the static part of the curve, however, the simulation underestimates the measurement.

The observed deviations between simulated and measured results can be explained by electromagnetic coupling effects, which are not encountered in the actual SEED model, i.e. effects related to crosstalk or electromagnetic radiation from the ESD generator relay. In this situation, the maximal current measured at the IC I/O pin(s) may be destructively attenuated due to coupling effects between the ESD gun and test board components like board traces, the CMT network or the CMC.

To minimize these effects, additional effort could be put into improving the shielding of the board from the direct impact of the relay (here, the ESD generator has not been shielded against the DUT). Also, to improve the modelled behaviour of the system an S-parameter model of PCB may be added to the SEED model.

Despite these deviations, the proposed SEED model has proved to be a good solution for estimation of the overall system transient response under ESD conditions. Furthermore, it can be used to predict system-level ESD robustness according to IEC61000-4-2 [12] and to evaluate IC robustness according to JEDEC-HBM [11] requirements. It also allows the impact of variations in the system and external ESD protection device parameters to be studied, to achieve optimal protection of the system IC while minimizing engineering and verification time.

9.2.10 Quasi-static model of ESD protection device with snap-back in VerilogA

VerilogA is a hardware programming language for analog circuits that uses a reduced instruction set from Verilog-AMS (analog mixed signal). VerilogA can be used to implement behavioral models of physically complex electronic components like ESD protection devices with snap-back, which are often based on the combination of advanced technologies of diodes, transistors or silicon controlled rectifiers (SCRs).

Quasi-static behavior is modelled by defining groups of I and V variables for inflection points in the IV curve. The position of these variables defines boundaries between device working regimes like the Vt1,It1-trigger point of the snap-back device and areas between to improve the accuracy of the model.

Calibration of the model can be easily achieved by tuning of these variables. The transition from one inflection point to another is described by linear or non-linear functions defined in VerilogA code. Figure 41 illustrates how the I-V curve can be subdivided and modelled with a set of I-V variables using VerilogA.

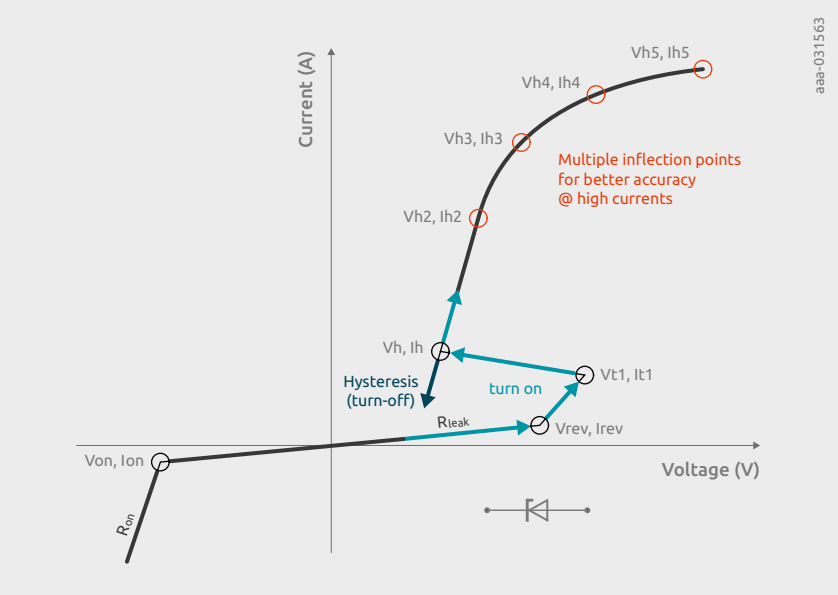

Figure 41 | Model of the quasi-static I-V curve of a uni-directional ESD protection device with snap-back showing variable groups placed into inflection points responsible for tuning of model working regimes.

As well as the quasi-static characteristics of the device, the hysteresis behavior which comes into play at device turn-off needs to be implemented in the model. In this case, the model will follow another IV curve definition. The unphysical overshoot which may occur by transition according to the initial IV curve will be prevented. Figure 42 shows this difference.

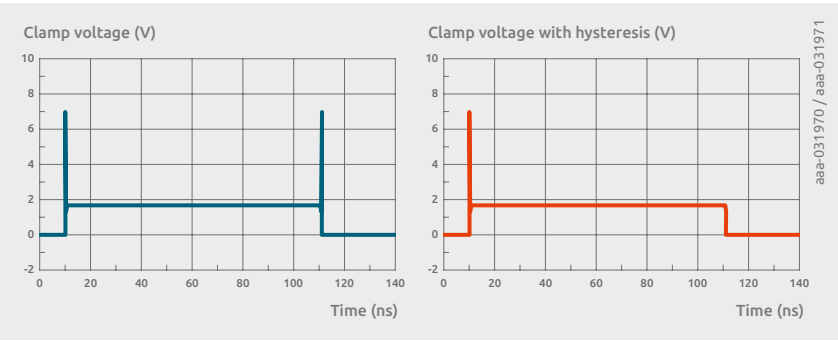

Figure 42 | The graphic on the left illustrates the unphysical voltage overshoot during turn-off of the snap-back ESD protection device. In the graphic on the right, this peak is compensated by implementation of hysteresis behaviour.

Another advantage of a VerilogA model is that it can be embedded inside other simulation programs like ADS and used for transient system-level analysis. The model itself can be further extended by connecting other discrete components to it. Although the addition of inductance will change the pure quasi-static model to semi-dynamic, this will only partly reflect the inductive voltage overshoot of the modelled device, since the snap-back delay is not implemented.

Full dynamic models are therefore needed to capture all dynamic effects as well as to get rid of some convergency problems related to abrupt slope change during snap-back in VerilogA and consequently be able to carry out more precise analysis of fast transient ESD events prior to steady state.

Example of quasi-static model implementation for a bi-directional ESD protection device with snap-back in VerilogA

```
//*****************************************************************
// SEED Quasi-static transient model of
// ESD protection device with snapback: PESD3V3Z1BSF
//
// Model working regions: leakage, snapback, linear and non-linear (self-heating)
// Additional effects: Hysteresis behaviour by turn-off of the device
//
// For further questions please contact:
// Sergej Bub
// System Level ESD Expert
// sergej.bub@nexperia.com
// Nexperia Germany GmbH
//*****************************************************************
//*
`include "constants.vams"
`include "disciplines.vams"
//*
//*****************************************************************
module PESD3V3Z1BSF_QSTM_M1(cathode, anode);
  inout cathode;
  electrical cathode;
  inout anode;
  electrical anode;
  parameter real Ron=0 from [0:inf);
  parameter real Von=0.8 from [0:inf);
  parameter real Vrev=6.3 from [0:inf);
  parameter real Rleak=1M from (0:inf);
  parameter real Vt1=8.22 from (0:inf);
  parameter real It1=0.13 from (0:inf);
  parameter real Vh=1.78 from (0:inf);
  parameter real Ih=0.272 from (0:inf);
  parameter real Vh2=4.8 from (0:inf);
  parameter real Ih2=22 from (0:inf);
  parameter real Vh3=11 from (0:inf);
  parameter real Ih3=30 from (0:inf);
  parameter real Vh4=55 from (0:inf);
```

```
  parameter real Ih4=35 from (0:inf);
  parameter real Vh5=727 from (0:inf);
  real Ion;
  real Irev;
  real Rdyn;
  real vout;
  real Iin;
  integer state;
  analog begin
    @(initial_step) begin
      state = 1;
      Ion = -Von/Rleak;
      Irev = Vrev/Rleak;
      Rdyn = Vh2/Ih2;
    end
    Iin = I(anode,cathode);
    @(cross(Iin-Irev,1)) state=1;
    @(cross(Iin-Ih,-1)) state=-1;
    vout = -Von+(Iin-Ion)*Ron;
    if (Iin>Ion) vout = Iin*Rleak;
    if (state>0) begin
      if (Iin>Irev) vout = Vrev + (Iin-Irev)*(Vt1-Vrev)/(It1-Irev);
      if (Iin>It1) vout = Vt1 + (Iin-It1)*(Vh-Vt1)/(Ih-It1);
      if (Iin>Ih) vout = Vh + (Iin-Ih)*Rdyn;
      if (Iin>Ih2) vout = Vh + (Iin-Ih)*Rdyn + (Iin-Ih2)*(Vh3/
      Ih2)*(1-limexp((Ih2-Iin)/Ih2));
      if (Iin>Ih3) vout = Vh + (Iin-Ih)*Rdyn + (Iin-Ih2)*(Vh3/
      Ih2)*(1-limexp((Ih2-Iin)/Ih2)) +
      (Iin-Ih3)*(Vh4/Ih3)*(1-limexp((Ih3-Iin)/Ih3));
      if (Iin>Ih4) vout = Vh + (Iin-Ih)*Rdyn + (Iin-Ih2)*(Vh3/
      Ih2)*(1-limexp((Ih2-Iin)/Ih2)) +
      (Iin-Ih3)*(Vh4/Ih3)*(1-limexp((Ih3-Iin)/Ih3)) +
      (Iin-Ih4)*(Vh5/Ih4)*(1-limexp((Ih4-Iin)/Ih4));
    end
    if (state<0) begin
      if (Iin>Irev) vout = Vh + (Iin-Ih)*Rdyn;
    end
    V(anode,cathode) <+ vout;
  end
endmodule
//****************************************************************
module PESD3V3Z1BSF_QSTM_M2(cathode, anode);
Here, the same code from module "PESD3V3Z1BSF_QSTM_M1" is used. To
describe the asymmetrical I-V curve of the bidirectional ESD
protection device with snapback, different values should be assigned
to the parameters of the module M2. For symmetrical case, all
parameter values should be kept in module M1.
endmodule
//****************************************************************
```


References

[1] OPEN Alliance, "IEEE 1000BASE-T1 EMC Test Specification for ESD Suppression Devices", Version 1.0, date 27.10.2017. Available online: http://www.opensig.org/download/document/216/OA+100Base-T1_ESD+device+Test+Specification+v1.0_11_17.pdf

[2] JEP 161. "System level ESD part 1: Common Misconceptions and recommended basic approaches." Arlington, VA, USA: Jan. 209.4.

[3] JEP 162. "System level ESD part 2: Implementation of effective ESD Robust designs." Arlington, VA, USA: Jan. 2013.

[4] S. Bub, J. Preibisch, J. Schütt, S. Holland, and A. Hilbrink, "Efficient prediction of ESD discharge current according to OPEN Alliance 100BASE-T1 specification using SEED", 16th ESD Forum in Dresden, 2019.4. Available online: https://assets.nexperia.com/documents/white-paper/Nexperia_Whitepaper_ESD_Discharge_Current_Measurement_Using_SEED_1.pdf

[5] G. Notermans, S. Bub, and A. Hilbrink, "Predicting system level ESD performance", 32nd Conference on Modelling and Simulation, 2018.

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Chapter 10

Packages and Quality

10.1 Packages for ESD protection devices

Nexperia offers a wide range of package solutions for ESD protection devices. In this handbook we will focus on the various package families and their technological characteristics. To make the right choice of product package it is important to match the application requirements with the technological characteristics of the package. In the following sections we will introduce the package families that are available and focus on this relationship.

The Nexperia website nexperia.com has a Selection Guide and a Package Catalogue to help you choose the right product package.

10.1.1 Application requirements and solutions

We can roughly break up the application requirements for an ESD protection device into four areas:

- Electrical requirements like the level of ESD robustness, the parasitic inductance and capacitance of the product in high-frequency applications, the breakdown voltage etc.
- Geometrical requirements for the package outline to fit into the application; for example, available space on PCB, single or multiline protection, PCB routing etc.
- Resilience of the product against environmental conditions, known as 'ruggedness' and reflected in different sets of reliability test requirements for product release and the corresponding release grades.
- Processability in the board assembly line at the customer side.

In contrast to many other application areas, such as power applications, heat dissipation is not part of this list of factors of first-order importance.

Let's start by reviewing the various package families and their pros and cons regarding these requirements.

10.1.2 Leaded versus leadless packages

Looking at the outer appearance of a product, apart from size the electrical interface of the product package is the most obvious differentiator. As the size of the package depends strongly on the electrical interface, we will use the interface as the first-order differentiator.

We distinguish between leaded and leadless packages. Leaded packages are – historically – the oldest form of surface-mounted devices (SMDs). They require relatively large areas on the PCB and due to their comparatively large electrical parasitics, they have some limitations in many modern (e.g., high frequency) applications. Hence, as the trend is towards higher densities on PCBs (miniaturization) and higher frequencies in applications, new packages for ESD applications are mainly realized as leadless package outlines. Figure 1 gives an impression of the evolution from larger to ever smaller packages and Figure 2 shows some examples of leaded and leadless packages.

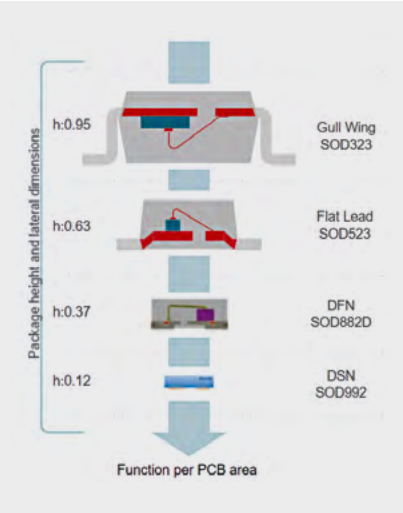


Figure 1 | Miniaturization of functionality reflected in the evolution of package form factors

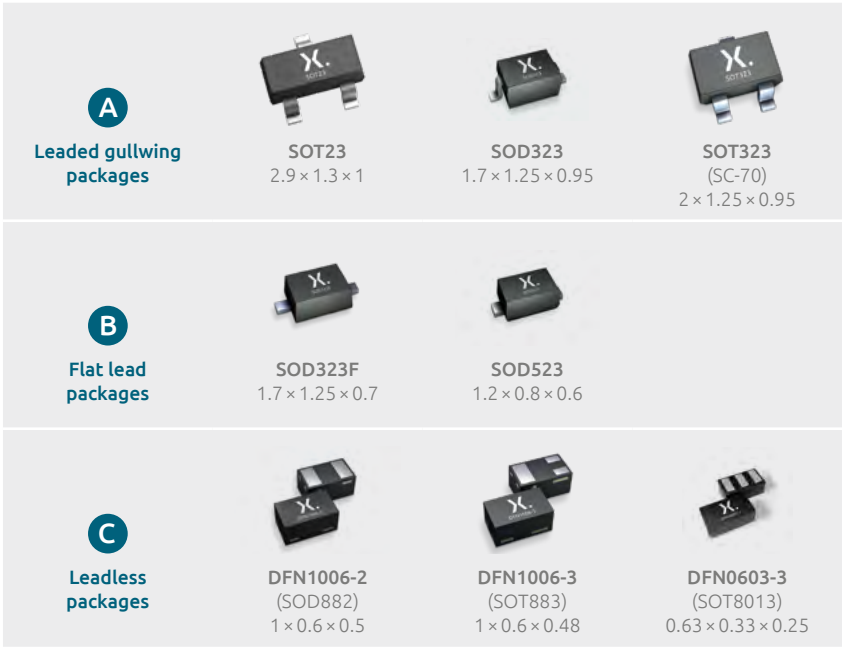


Figure 2 | Examples of leaded and leadless packages

Leaded packages

Development of surface-mounted devices for discrete semiconductors began in the 1960s and in 1969 the SOT23 package was introduced which is still produced in large quantities. Since then, many more leaded packages have been released. Due to their relatively large sizes and pitches (lead-to-lead distances) the requirements to handle these packages in the board-mounting process are quite low. All leaded packages which Nexperia offers for ESD protection applications are suitable for wave soldering as well as the reflow solder technology that is standard today.

The packages show a very good ruggedness but due to their high parasitic inductances and capacities they are not suitable for high-frequency applications like, for example, the protection of high-frequency data lines. Further, with the increasing functional density in many modern applications the need for miniaturization is ever increasing. In these cases, the leadless package families offer solutions.

Gullwing packages

The first discrete semiconductor package in surface mount technology (SMT) to enter the market, the SOT23, is also a gullwing package. (The term 'gullwing' metaphorically describes the special bending of the leads.) Today, we have a large family of packages with gullwing leads. The architecture of these packages follows a quite simple approach. There are relatively thick layers of mold compound above and under the leadframe which carries the silicon die on the die pad. This causes quite large package heights but improves the stability of the packages against outer forces.

The long bend leads provide improved flexibility against bending of the PCB and thermal expansion, and the solder connections are large and strong. These are advantages in board-level reliability. However, the leads and long internal wire connections cause high values in parasitic inductance and capacitance, limiting the frequency range of the protected line.

Figure 3 shows some X-ray and light optical photos of the SOT363 package. Relative to the package orientation, the dies are assembled upside down.

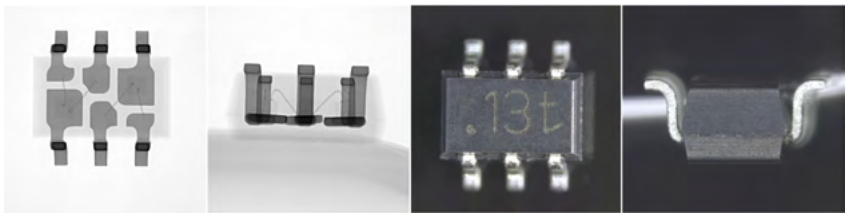


Figure 3 | X-ray and light-optical photos of the SOT363 gullwing package

Flat leaded packages

Flat leaded packages were introduced to reduce the height and lateral dimensions of leaded packages. The short leads emerge from the bottom of the package body without any bending. Compared to gullwing packages the electrical parasitics will be somewhat lower, which is also the case for the mechanical ruggedness of the package against board bending and thermal expansion. Figure 4 shows as an example our SOD323F package.

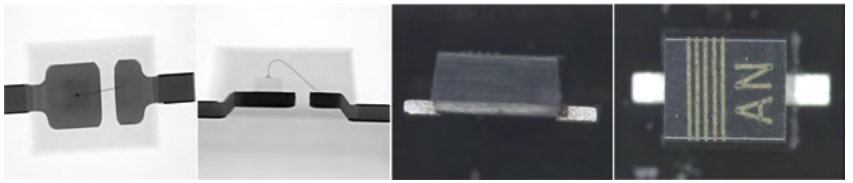


Figure 4 | X-ray and light optical photos of the SOD323F flat-lead package

Leadless packages: DSN and DFN packages

The increasing integration and miniaturization of electronic applications requires a reduction in package dimensions, usually in combination with improved electrical performance. Hence, the next step in package miniaturization was to move the electrical contacts of the packages from the package sides to underneath the packages. At Nexperia, we have recognized this trend with the introduction of a growing variety of DFN and DSN packages to our package catalogue.

DSN and DFN packages both have their solderable electrical interfaces, generally as pads underneath the product. DFN packages use mold compound as protection against the product environment and their construction might be based on completely different concepts, e.g. leadframe based, substrate based or even molded chip-scale. DSN packages are chip-scale packages without plastic encapsulation. At least at the package sidewalls, the semiconductor material is visible, and might be protected by an isolating thin layer of deposited material (protected DSN). We call a package a chip-scale package if the package area is not greater than 1.2 times the die area and it must be single-die.

Unprotected DSN packages

The simplest architectural approach for a package is to apply solderable contact pads directly to the semiconductor crystal. These pads are created from electro-plated Cu/Sn layers, or from electroless plated Ni(Pd)Au layers. The front side (contact side) of these products is passivated around the pads and electrically isolated by the passivation layers of the diffusion process. For the electroplated

products an additional layer of polyimide is applied. The back side of the product is optionally coated with a mold foil. Very small package outlines can be realized (Figure 5 shows some examples).

From a package point of view, this construction offers extremely low values for parasitic capacitances and inductances. The thermal coupling to the PCB is quite good due the large pads with their direct contact to the active silicon. For the protection of battery-powered lines, it is important to realize that the sidewalls of these products are formed by unpassivated silicon; any solder on these sidewalls should be avoided because it might cause high ohmic leakage currents. This should be reflected in the footprint layout on the application PCB and the solder amount (i.e. stencil openings and stencil thickness) used for these products.

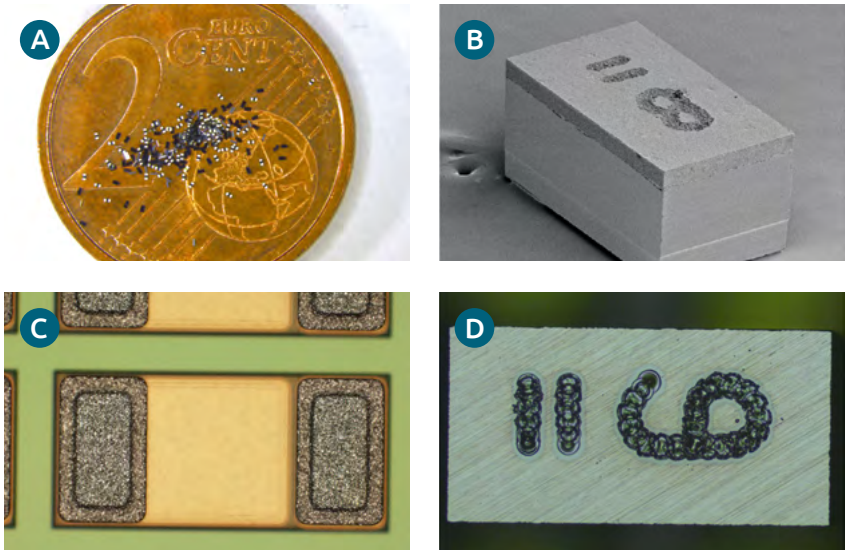


Figure 5 | Some examples of unprotected DSN products: A DSN0402 products on a 2-€Cent coin, B a DSN0603 product with the optional mold foil on the backside, C the contact pads of a DSN0603 product, D the backside of a DSN0603 product without the optional mold foil and laser marking on bare silicon.

Protected DSN packages

The basic construction of these packages is the same as for unprotected DSN packages, except that the complete product surface (apart from the contact pads) is passivated using an atomic layer deposition technique.

For this package family there is no optional back side coating with mold foil available.

Leadframe based DFN packages

Leadframe based DFN packages provide the high robustness of leadframe based plastic packages on a much smaller footprint compared to leaded packages. Furthermore, many packages in this family offer exposed die pads which can be soldered to a heatsink on the PCB for improved thermal performance. Compared to leaded packages the electrical parasitics are improved but do not reach the top performance level of DSN packages. Usually, wire bonding is used for the electrical connection of the silicon to the leadframe. Depending on the application requirements on the PCB, the same semiconductor die can be offered in a choice of different leadframe based packages, as shown in Figure 6, which also illustrates the miniaturization effect of moving from leaded to DFN packages.

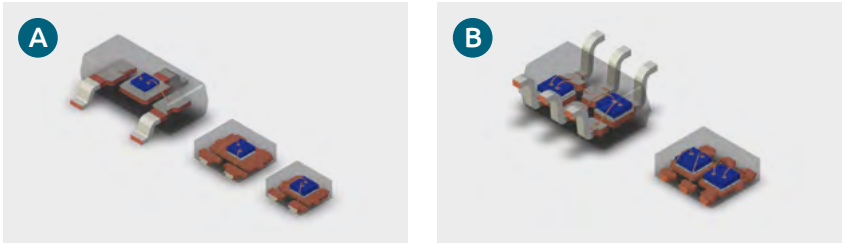


Figure 6 | The same semiconductor die in different leadframe based packages will deliver the same basic functionality adapted to the application requirements on the PCB. A SOT23 – SOT8009 – SOT8015. B SOT363 – SOT1268. For the DFN packages the required area on the PCB is largely reduced

Substrate based DFN packages

The outer appearance and footprint of substrate based DFN packages are very similar to leadframe based DFN packages. The difference between the two families is the internal package architecture. For the substrate based packages a small piece of PCB (the substrate) is used to carry the semiconductor die(s) and to realize the external contact pads instead of a metal leadframe. As well as various routing opportunities and hence a flexible approach for product and internal die footprints, this technology is also able to realize the same functionality on a smaller package area compared to leadframe based DFN. Even chip-scale dimensions are possible if flip-chip die mounting is applied.

For discrete semiconductor products the substrate is usually a PCB with two metal (Cu) layers; one to form the outer contact pads and the other to provide the internal contact pads for the connection to the semiconductor die(s). Both layers are connected by vias (Cu filled through-holes). As well as wire bonding, the substrate-based architecture is also perfectly suitable for flip-chip die mounting which will, for example, reduce the parasitic inductance of the product. This can be

realized by, for example, applying an electroplating bump process to the wafers after diffusion in which contact pillars are grown on the contact pads of the semiconductor device. Figure 7 shows an example of such devices after bumping.

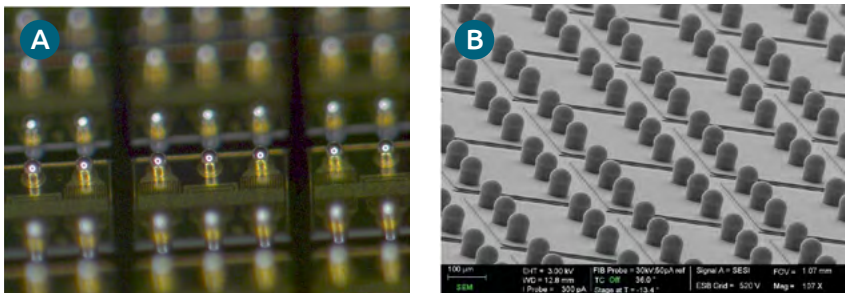


Figure 7 | Semiconductor devices with electroplated Cu/Sn pillar bumps under a light microscope A and in a SEM B

The singulated devices are placed upside down (flipped) onto the corresponding contact pads of the PCB substrate, soldered by a reflow step and finally the construction is molded with a plastic mold compound. An example of this architecture is shown in Figure 8.

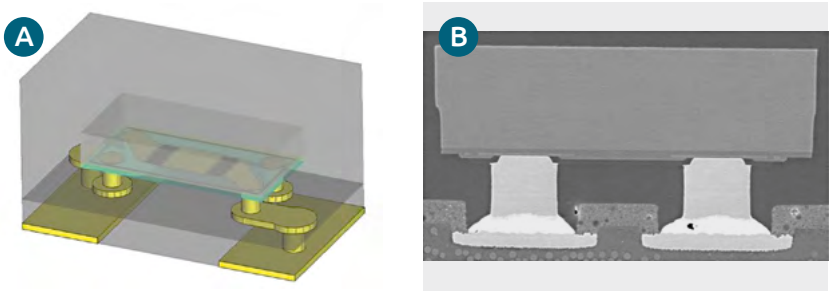


Figure 8 | The basic architecture of a flip-chip LGA package A. The die is flipped with its contact pillars onto the two-layer PCB and surrounded by mold compound. A SEM cross section of this construction is shown in B

DFN chip scale packages: molded DSN packages

Our DFN chip scale packages are based on the DSN products described above. Instead of electroplated Cu/Sn pads, electroplated Cu/Ni pads are used with a thin Au flash on top.

All sides except the back side of the product (and, of course, the contacts) are overmolded with a thin epoxy mold layer. The product back side is protected by a mold foil. Hence, there is full six-side plastic protection for these packages. This technology offers a combination of the high ruggedness of plastic packages and the extremely low electrical parasitics of DSN packages. Figure 9 shows our SOD972E (DFN0603-2) and SOT8013 (DFN0603-3) packages as examples of molded DSN packages.

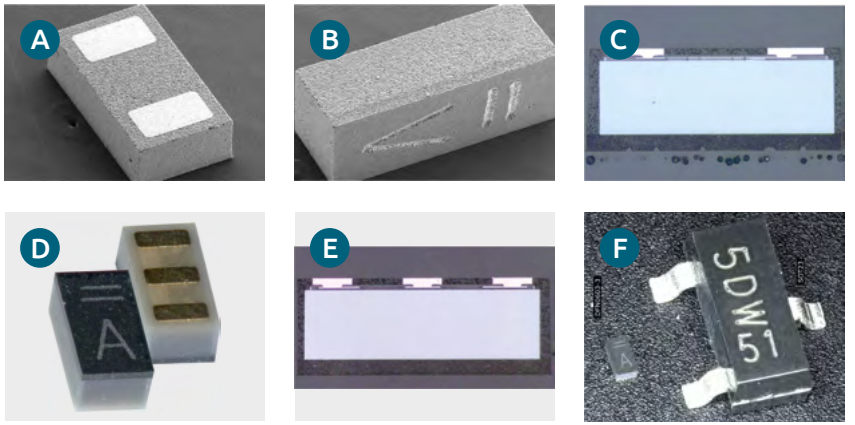


Figure 9 | Examples of molded DSN packages. The interface side and the four sidewalls are protected by an epoxy mold plastic, the back side with the marking is formed by a mold foil. SOD972E: SEM photos of the contact side A, the sidewall and backside B and a cross-section C are shown. SOT8013: A view under the light microscope D, a cross section E and a size comparison with the SOT23 package F

Side-wettable flanks

Looking at the standard versions of DFN packages, the solderable areas of the contact pads are underneath the package. For selected package types we additionally offer package outline versions with side-wettable flanks. For these versions, the solderable areas are extended to the sidewalls of the package. This will lead to the formation of a solder meniscus after a proper PCB soldering process. The solder menisci can be easily controlled by using automated optical inspection to confirm the quality of the soldering. This package option is used for high-reliability applications, such as in the automotive industry. Figure 10 shows two different realizations of side-wettable flanks for leadframe-based DFN packages and Figure 11 illustrates the significant advantage of side-wettable flanks with regard to the detectability of cold solder joints by (automatic) optical inspection.

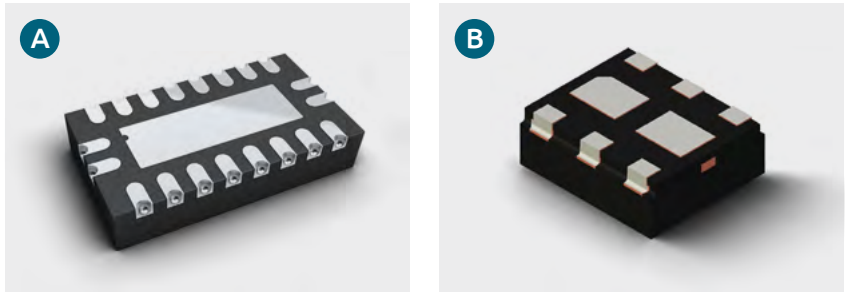


Figure 10 | Two examples of how side-wettable flanks can be realized for DFN packages: A by dimples in the leadframe and B by step-cut sawing of the package

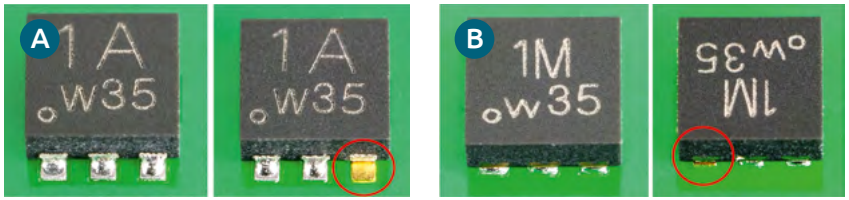


Figure 11 | Optical detectability of a cold solder joint with side-wettable flanks and an appropriate solder footprint A and without side-wettable flanks B

10.1.3 Wafer level chip scale packages

Our wafer level chip scale products use arrays of pre-formed solder spheres as the connecting interface to the PCB. The products are not molded, hence the lateral dimensions are the same as those of the silicon die and the package body is bare silicon. Optionally, some products are also available with a mold foil coating on the back side. These products are mainly used for multi-line ESD protection in mobile devices. Figure 12 shows some basic examples of WLCSP package constructions.

Figure 12 | Examples of wafer level chip scale packages. A WLCSP4 package outline A, a WLCSP15 package with the solder balls on the contact side and the bare silicon body B and a WLCSP15 package with the optional back side coating mold foil C

Common mode filters with integrated ESD protection

Our product family of common mode filters with integrated ESD protection functionality is designed to protect the most advanced data interfaces which operate at very high frequencies. The devices are designed to provide low insertion loss for differential high-speed signals on each channel while unwanted common mode signals are attenuated. This is realized by integrated coils. In addition, the channels are protected against ESD. The products combine highest performance with excellent compactness. Some examples are shown in Figure 13.

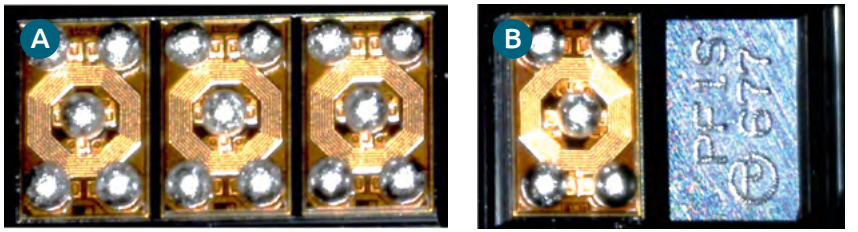


Figure 13 | Common mode filter products with integrated ESD protection for ultra-fast data lines. These products are available in different configurations in a WLCSP5-, WLCSP10- or WLCSP15-package for the protection of one, two or three differential data lines. The photo A shows the contact side of the WLCSP15 product in which the integrated coils to achieve outstanding filter performance on a very small footprint are clearly visible. Picture B shows the WLCSP5 product from contact side and back side with the laser marking in the silicon

10.1.4 Clip flat power packages

Clip flat power (CFP) packages are a special form of leadframe based packages, designed to offer low electrical resistance and high heat dissipation. Due to these characteristics, they are used in power applications. In the area of ESD protection, some transient voltage suppression (TVS) diodes use these packages as they have to carry some power over a longer time.

There are CFP package outlines on the market with and without leads, for TVS diodes with flat leads. Leadless packages are sometimes used for power MOSFETs. For power MOSFETs there are also many package designs with top or bottom heatsinks available.

The special design feature of CFP packages is the use of copper clips instead of bond wires for the electrical connection between the power-carrying pins and the silicon. The clips significantly lower the electrical and thermal resistance. The parasitic inductance is also slightly improved compared to using bond wires.

Figure 14 shows the basic construction of a clip flat power package using the example of a SOD123W (CFP3) package which has been decapsulated in our lab.

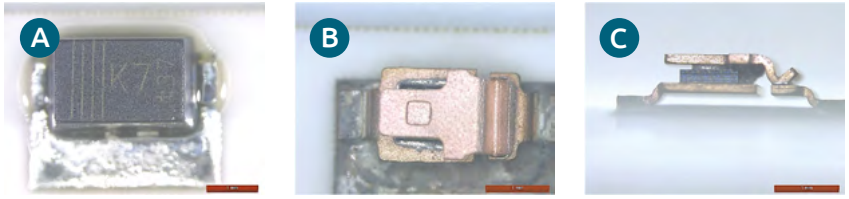


Figure 14 | The SOD123W (CFP3) package as an example of a clip flat power packages. A shows a product soldered on a lab carrier and the same product with the plastic body removed can be seen in B from the top and from the side C. The basic construction principle of CFP packages becomes visible

10.2 Failure symptoms in electronic components caused by ESD and surge events

ESD is a significant problem for the semiconductor industry, during production and especially in use. It can be the main cause of customer complaints and this section looks at typical ESD failures in the field.

Nexperia's quality team has created a library that categorizes ESD failures.

The observed ESD fail behavior in products returned from the field can be subdivided in categories as shown in Table 1.

Most fails can be distinguished from each other by their category, but sometimes combinations may appear.

Table 1: Categories for ESD fails

Categories for ESD fails
Burnt wire
Burn mark on die
Package crack
Burn mark on package
Burnt resistor
EB flashover
Burn mark below ball
Carbonized mould
Movable charges
Round burn mark in active area
Hot spot

Examples of typical ESD field failures for different category:

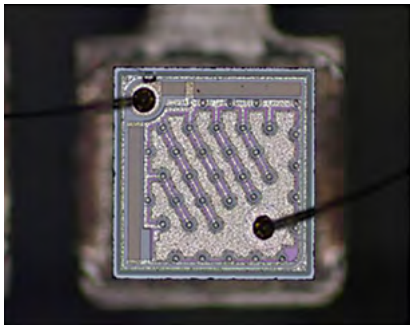
Burnt wire

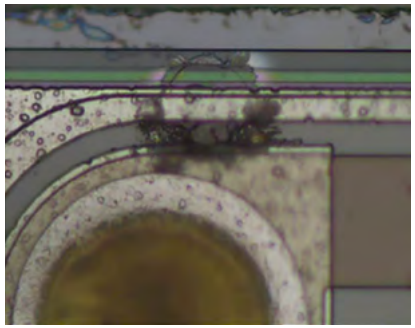
An X-ray image of a typical burnt wire is shown below. Sometimes even traces of the burnt wire can still be observed in the X-ray.

Conditions: VZ_Surge_200 us, V_{cap} = 20 V, were applied to collector – base by surge tester. The device failed after approximately 200 µs. At the point of failure a current of approximately 15 A passed through the device.

Burn mark on die

A typical image of a burn mark on die is shown below.





To create this fail behavior, the following conditions were applied:
ESD HBM, 1 positive pulse, 9 kV applied to collector – base.

Package crack

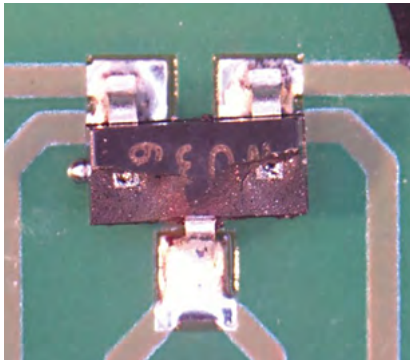
A typical image of a package crack is shown on the right.

Conditions:
V_{EB} = 2 V, V_{CE} = 13 V,
t = approximately less than 5 sec

Burn mark on package

An image of a burn mark on package is shown on the right.

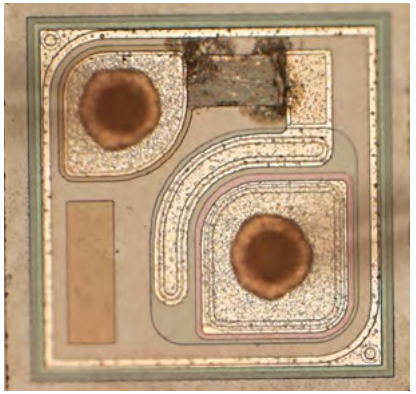
Conditions: VZ_Surge_50 us, V_{cap} = 100 V, were applied to collector – base by surge tester. The device failed after approximately 50 µs. At the point of failure, a current of approximately 17 A passed through the device.



Burnt resistor

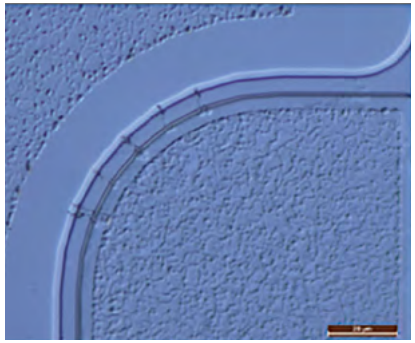
A typical image of a burnt resistor is shown on the right.

To create this fail behavior, the following conditions were applied:
ESD HBM, 1 positive pulse, 2.8 kV applied to collector – base.



Emitter-Base flashover

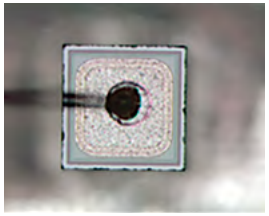
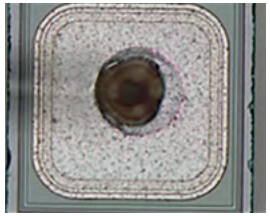
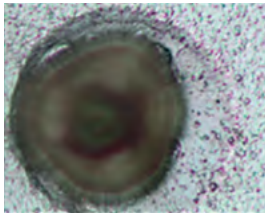
A typical image of an Emitter-Base flashover is shown below.

To create this fail behavior, the following conditions were applied: ESD MM, four times, starting with 250 V applied and followed by three incremented steps with 25 V more applied to emitter – base each time. Each time three pulses (positive and negative) have been applied.

Burn mark below ball

An image of a burn mark below ball is shown below.

Conditions not available.

Carbonized mould

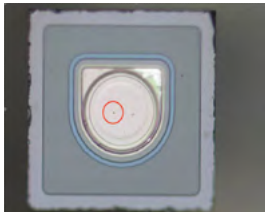
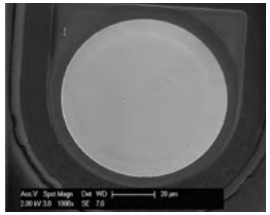
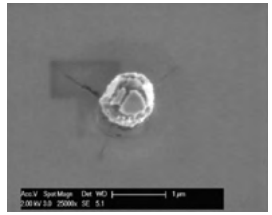
No Image available.

Movable charges

Movable charges is a failure that cannot be seen in an image.

Round burn mark in active area

A typical image of a round burn mark in an active area is shown below.

To create this fail behavior, following conditions were applied: ESD HBM, one time, 8 kV applied to collector – base

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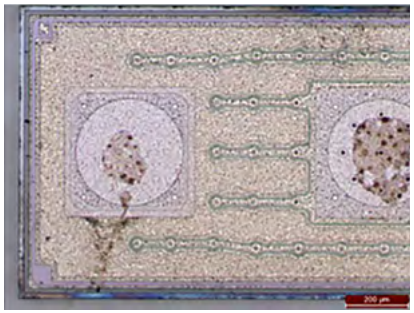
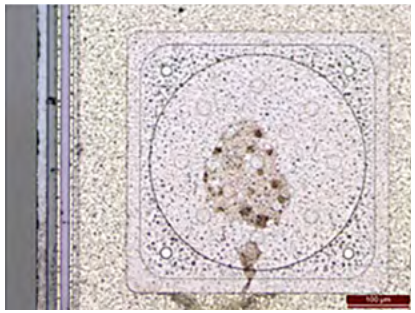
Hot spot

A typical image of a hot spot in an active area is shown below.

Conditions: Surge_100 us, V_{cap} = 22.5 V, were applied to collector – base by surge tester. The device failed after approximately 100 µs. At the point of failure, a current of approximately 36 A passed through the device.

Generally, an EOS or ESD damage is caused by a pulse that exceeds the devices limiting values. The parameters of such a pulse are shape, duration, voltage peak and current peak. Furthermore, it can be a single pulse or a repetitive pulse (with varying frequency). An immense variety of possible pulses can be experienced in use. Such variations can lead to slightly different failure pictures as seen in our simulations compared to failures in the field.

Chapter 11
Summary

Semiconductor devices are constructed with microscopic oxide layers, making them susceptible to everyday electrostatic discharge (ESD) events. As semiconductor geometries continue to shrink, the sensitivity of individual integrated circuits (ICs) and data lines to transient voltage pulses and current surges increases, leaving complete systems more vulnerable to ESD. Internal structures offer basic protection against ESD events typically encountered during production and manufacturing. However, to withstand ESD events likely to occur in the field, such as high pulse voltages up to 30 kV (peak) and longer duration current surges (~60 µs), additional external ESD protection devices are essential.

It is crucial that these external ESD protection devices do not compromise system performance. With electronic components playing a critical role in data communications, modern high-speed data interfaces now operate with reduced voltage levels and at very high data rates (tens of Gbit/s). Therefore ESD protection devices guarding these transceiver interfaces cannot negatively impact on signal integrity, otherwise data could be lost or corrupted.

Nexperia, with a long-standing history in designing and manufacturing ESD protection devices, offers the highest level of protection in the industry's smallest packages, with minimal impact on signal integrity. This handbook provided insights into the physical layers of various data interfaces across mobile, computing, consumer, and automotive applications, to assist readers in the selection of appropriate ESD protection topologies for structures of different drivers and receivers and their signal levels.

Chapter 2 of this handbook reviewed the fundamentals of ESD, sources of ESD events and the symptoms of ESD failures in electronic circuits.

Chapter 3 discussed the principles of ESD protection and presented various approaches tha for protecting electronic devices against ESD and surge events including diodes, varistors and others, while the most relevant datasheet parameters for ESD protection devices and their importance for ensuring properly functioning interfaces were described in Chapter 4.

Chapter 5 considered the relevant testing standards for ESD and surge protection including IEC61000-4-2, ISO10605, IEC61000-4-4 and others. Also addressed in this chapter were test procedures for ensuring compliance with ISO standards for immunity to transients on voltage supply lines for automotive electronic control units.

Chapter 6 analysed radio frequency (RF) measurements, signal integrity, and testing methods for ESD protection devices, including a deep dive into s-parameters, PCB de-embedding, and T-checks. It also discussed the impact of ESD protection devices on high-speed serial interfaces, compliance testing in addition to layout and routing of ESD protection devices for optimizing signal integrity.

Chapter 7 looked at the operation of and requirements for protecting some commonly used data interfaces like USB and PCIe as well as video interfaces such as HDMI and MIPI(D-PHY, M-PHY, C-PHY). It also discussed topologies for protecting industrial and automotive Ethernet network interfaces operating at various data rates from 10 Mbps up to several Gbps using different cables as well as automotive applications like FPD-link, APIX and GMSL. This chapter also reviewed requirements for protecting RF antennae against ESD.

Chapter 8 presented a latch-up analysis for deep-snap back devices and showed how electromagnetic interference (EMI) scanners can be used in time-domain ESD analysis.

Chapter 9 covered whole system modeling of the signal pathway from the external connector to the protected IC, including internal and external ESD protection devices, the PCB itself and other discrete components. Using SPICE models for s-parameter analysis of how ESD devices affect signal integrity was also considered. Furthermore, this chapter introduced the system efficient ESD design (SEED) methodology for simulating the behavior of ESD protection devices and system chip interfaces, both as individual blocks and in combination.

Finally, Chapter 10 focused on Nexperia's extensive range of package options for ESD protection devices and presented guidelines for making the right choice of product package by matching the application requirements with the technological characteristics of the package.

For questions and suggestions do not hesitate to contact us at:
www.nexperia.com/about/worldwide-locations/sales-offices

Abbreviations

ADAS	Advanced driver assistance systems
ADC	Analog/digital converter
ADS	Advanced Design System
AOI	Automated optical inspection
APIX	Automotive Pixel Link
BER	Bit Error Rate
CAN	Controller Area Network
CCCS	Current controlled current source
CCW	Counterclockwise
C_d	Diode capacitance
CEC	Consumer electronics control
CM	Conductivity modulation
CMC	Common-mode choke
CMT	common-mode termination
C_t	Tip capacitance
CW	Continuous wave / clockwise
DC	Direct current
DDC	Display data channel
DFP	Downstream forcing port
DP	Display Port
DPI	Direct power injection
DUT	Device under test
DVD	Digital versatile disk
ECU	Electric control unit
EDID	Extended display identification data
EFT	Electrical fast transients
EMC	Electromagnetic compatibility
EMI	Electromagnetic interference
EOP	End-of-packet
EOS	Electrical overstress
ESD	Electrostatic discharge
f_{-3dB}	Frequency with -3dB attenuation, loss
FET	Field-effect transistor
FPD-link	Flat Panel Display Link
FRL	Fixed Rate Link
GND	Ground
GPS	Global Positioning System
GSM	Global System for Mobile Communication
HBM	Human Body Model
HDCP	High-bandwidth Digital Content Protection
HDMI	High Definition Multimedia Interface
HMM	Human Metal Model
HS	High speed
IC	Integrated circuit
I_{hold}	Hold current
IoT	Internet of Things
I_{PP}	Peak pulse current
I_{PPM}	Peak pulse current maximum, single pulse
I_{RM}	Leakage current at VRWM
IVN	In-vehicle network

LIN	Local Interface Network
LS	Low speed
LVDS	Low-voltage differential signal
MC	Mode conversion
MDI	Media dependent interface
MIPI	Mobile Industry Processor Interface
ML	Main Link
MOSFET	Metal oxide field-effect transistor
NFC	Near field communication
NRZ	Non return to zero (code)
NRZI	Non return to zero inverted (code)
PCB	Printed circuit board
PCIe	Peripheral Component Interconnect Express
PD	Power delivery
PLL	Phase-locked loop
PoA	Power-over-APIX
PoC	Power-over-Coax
PoDL	Power-over-Data-line
PoE	Power-over-Ethernet
P_{pp}	Peak pulse power
RD	Running disparity
R_{dyn}	Dynamic resistance
RF	Radio frequency
RX	Receiver input
S_{11}	Return loss
S_{21}	Insertion loss
SBC	System basis chip
SBU	Sideband usage
SCR	Silicon controlled rectifier
SEED	System Efficient ESD Design
SerDes	Serializer/Deserializer
SoC	System-on-Chip
S-parameters	Scattering parameters
SPICE	Simulation Program with Integrated Circuit Emphasis
STP	shielded twisted-pair
SWCAN	Single-wire CAN
T_{amb}	Ambient temperature
T-Box	Telematic box
TDR	Time Domain Reflection
T_j	Junction temperature
TLP	Transmission-line pulse
TMDS	Transmission minimized differential signaling
TP	Test point
TPA	Test point adapter
T_{stg}	Storage temperature
TTL	Transistor-transistor logic
TVS	Transient voltage suppressor
TX	Transmitter output
UFP	Upstream forcing port
UI	Unit Interval
USB	Universal Serial Bus
UTP	Unshielded twisted-pair

V2X	Vehicle to anything
V_{BR}	Breakdown voltage
V_{CL}	Clamping voltage
VCVS	Voltage controlled voltage source
VDM	Vendor defined massages
V_{ESD}	Maximum ESD voltage, robustness
V_F	Forward voltage
VF-TLP	Very fast TLP
V_{hold}	Hold voltage
VPN	Virtual private network
V_{RWM}	Stand-off voltage, max. operation voltage
WiFi	Wireless local area network (artificial abbreviation)
XOR	Exclusive OR, logical function

Appendix

15.1 Mobile, computing and consumer applications

USB Interfaces

This USB section of the appendix proposes products for protecting USB data signal lines and auxiliary signal lines, excluding VBUS. For VBUS protection options refer to the power line protection section of this appendix.

USB2.0

The USB2.0 connection with a Type A und Type B connector includes one differential pair for the High speed (480 Mbit/s) data with the signal lines D+ and D–. Furthermore a 5 V VBUS and a Ground connection is present. For the Micro-B and Mini-A connectors an additional signal (ID) is provided.

Table 1: Product proposals for USB2.0 D+/D– signal lines

Signal name	Type name	V_{RWM}	C_d(typ)	I_{PPM} for t_P = 8/20 µs	Package name	Number of lines
D+/D–	PESD3V3F1BSF	3.3 V	0.78 pF	20 A	DSN0603-2 (SOD962)	1
	PESD5V0C1ULS(-Q)	5 V	0.6 pF	6.5 A	DFN1006BD-2 (SOD882BD)	1
	PESD5V0C2UM(-Q)	5 V	0.5 pF	6.5 A	DFN1006-3 (SOT883)	2
	PESD4V0X2UM	4 V	0.82 pF	1.5 A	DFN1006-3 (SOT883)	2
	PESD15VW1UCSF	15 V	1 pF	18.5 A	DSN0603-2 (SOD962)	1
	IP3319CX6	5 V	1.5 pF (CMF)	7.5 A	WLCSP6	2 + 1 (ID)
ID	PESD5V0S1BL(-Q)	5 V	152 pF	12 A	DFN1006-3 (SOT883)	1
	PESD5V0S1USF	5 V	35 pF	3.5 A	DSN0603-2 (SOD962)	1

USB3.2 Gen 1

This USB standard works with a lane speed of 5 Gbit/s on the SuperSpeed RX and TX lines. For the protection of D+ and D– lines products listed in Table 1 can be applied but also the products from Table 2 for keeping the bill of materials (BOM) simple. Recommendations given in Table 2 for CC and SBU lines also apply to all other USB versions. Devices with a V_{RWM} rating below or equal to 3.3 V should be placed behind the DC-blocking capacitors. Devices with V_{RWM} larger than 5 V can be placed at the connector.

Table 2: Product proposals for USB3.2 Gen 1

Signal name	Type name	V_{RWM}	C_d	I_{PPM} for t_P = 8/20 µs	Package name	Number of lines
RX, TX	PESD3V3Z1BCSF	3.3 V	0.45 pF	15 A	DSN0603-2 (SOD962)	1
	PESD4V0W1BCSF	4.0 V	0.55 pF	20 A	DSN0603-2 (SOD962)	1
	PESD5V5X1BCL(-Q)	5.0 V	0.49 pF	1.7 A	DFN1006-2 (SOD882)	1
	PESD3V3C2UM	3.3 V	0.4 pF	6.5 A	DFN1006-3 (SOT883)	2
	PESD4V0Z2BCDF	4 V	0.31 pF	11 A	DFN0603-3 (SOT8013)	2
	PUSB3FS4	3.3 V	0.29 pF	6.5 A	DFN2510A-10 (SOT1176-2)	4
	PUSB3FR6	3.3 V	0.35 pF	7 A	DFN2111-7 (SOT1358-1)	6
	PCMFxUSB3S[1]	5 V	0.25 pF	7 A	WLCSP5, 10, 15	2,4,6
CC/SBU	PESD24VV1BSF	24 V	9.3 pF	4.7 A	DSN0603-2 (SOD962)	1
	PESD24VV1BL	24 V	14 pF	3.5 A	DFN1006-2 (SOD882)	1
	PESD30VV1BSF	30 V	4.8 pF	2.1 A	DSN0603-2 (SOD962)	1
	PESD5V0X1BCAL	5 V	0.85 pF	1.8 A	DFN1006-2 (SOD882)	1
	PESD5V0X2U-AM(B)-(Q)	5 V	0.8 pF	2.5 A	DFN1006(B)-3 (SOT883)	2

1) ESD protection with integrated common mode filter

USB3.2 Gen 2

USB3.2 Gen 2 operates at a lane speed of 10 Gbits/s. Consequently, the ESD protection device must possess a suitably lower capacitance.

Table 3: Product proposals for USB3.2 Gen 2

Signal name	Type name	V_{RWM}	C_d	I_{PPM} for t_P = 8/20 µs	Package name	Number of lines
RX, TX	PESD4V0Z1BSF	4 V	0.24 pF	9.5 A	DSN0603-2 (SOD962)	1
	PESD5V5C1BBSF	5.5 V	0.26 pF	8.1 A	DSN0603-2 (SOD962)	1
	PESD9V0Z1BDSF	9 V	0.32 pF	9 A	DSN0603-2 (SOD962)	1
	PESD15VW1BCSF	15 V	0.45 pF	20 A	DSN0603-2 (SOD962)	1
	PESD1V0Y1BIF	1 V	0.18 pF	6 A	DSN0603-2 (SOD962)	1
	PESD1V0R1BFSF	1 V	0.24 pF	8 A	DSN0603-2 (SOD962)	1
	PUSB3BB4	3.3 V	0.17 pF	6.5 A	DFN2510A-10 (SOT1176-2)	4
	PESD5V0C2BDF	5 V	0.21 pF	8 A	DFN0603-3	2
	PUSB3FA2	1.65 V	0.17 pF	7 A	DFN2510A-10 (SOT1176-2)	4
	PCMFxUSB3BA f_{-3dB} = 10 GHz [1]	4 V	0.3 pF	7.5 A	WLCSP5, 10, 15	2,4,6
	PCMFxUSB3B/C f_{-3dB} = 8.1 GHz [1]	4 V	0.3 pF	9.5 A	WLCSP5, 10, 15	2,4,6

1) ESD protection with integrated common mode filter

USB 4 Gen 3

With USB4 Gen 3 the data rate is doubled again to 20 Gbit/s per lane. Only certain protection devices with low-inductance packages like SOD962 offer the required RF performance for this application.

Table 4: Product proposals for USB4 Gen 3

Signal name	Type name	V_{RWM}	C_d	I_{PPM} for t_P = 8/20 µs	Package name	Number of lines
RX,TX	PESD5V0Y1BCSF	5 V	0.16 pF	6 A	DSN0603-2 (SOD962)	1
	PESD4V0Y1BCSF	4 V	0.16 pF	5.5 A	DSN0603-2 (SOD962)	1
	PESD1V0C1BSF	1 V	0.18 pF	6.5 A	DSN0603-2 (SOD962)	1
	PESD1V0Y1BBSF	1 V	0.16 pF	5.5 A	DSN0603-2 (SOD962)	1
	PESD1V0H1BSF	1 V	0.15 pF	5 A	DSN0603-2 (SOD962)	1
	PESD1V0R1BDSF	1 V	0.1 pF	4.8 A	DSN0603-2 (SOD962)	1
	PESD1V0R1BCSF	1 V	0.085 pF	3.5 A	DSN0603-2 (SOD962)	1

HDMI Interfaces

Table 5: Product proposals for HDMI

Signal name	Type name	V_{RWM}	C_d	I_{PPM} for t_P = 8/20 µs	Package name	Number of lines
TMDS/ FRL	PHDMI2AB4	5 V	0.17 pF	7 A	DFN2510A-10 (SOT1176-2)	4 (HDMI2)
	PHDMI2FR4	5 V	0.29 pF	7 A	DFN2510A-10 (SOT1176-2)	4 (HDMI1)
	PCMFxHDMI14S[1]	5 V	0.25 pF	7 A	WLCSP5, 10, 15	2, 4, 6; (HDMI1)
	PCMFxHDMI2BA[1]	4 V	0.3 pF	7.5 A	WLCSP5, 10, 15	2, 4, 6; (HDMI2)
	PESD5V5C1BBSF	5.5 V	0.26 pF	8.1 A	DSN0603-2 (SOD962)	1
CEC	PESD5V0S1BL(-Q)	5 V	35 pF	12 A	DFN1006-2 (SOD882)	1
DDC (I^2C)	PESD5V0V1BL(-Q)	5 V	11 pF	4.8 A	DFN1006-2 (SOD882)	1
HEC	PESD5V0X1BCAL	5 V	0.85 pF	1.8 A	DFN1006-2 (SOD882)	1
Hot-plug	PTVS5V0Z1UCL	5 V	160 pF	44 A	DFN1006-2 (SOD882)	1

1) ESD protection with integrated common mode filter

15.2 Automotive Applications

USB Interfaces

For automotive applications special aspects for the package technology are important. For a very robust mounting with higher sheer forces and the capability of AOI (Automatic Optical Inspection) customers prefer leadless packages with the feature of side wettable flanks (SWF) and if possible plastic leadless packages (DFN types).

USB2.0

Table 6: Product proposals for USB2.0 D+/D– signal lines

Signal name	Type name	V_{RWM}	C_d(typ)	I_{PPM} for t_P = 8/20 µs	Package name	Number of lines	Comments
D+/ D–	PESD3V3F1BSF	3.3 V	0.78 pF	20 A	DSN0603-2	1	Smallest footprint
	PESD5V0H1BLL-Q	5	0.25 pF	6.5 A	DFN1006L-2	1	High speed optimized package
	PESD5V0H1BLG-Q	5 V	0.25 pF	6.25 A	DFN1006LD-2	1	High speed optimized package with SWF
	PESD5V0H2BFG-Q	5 V	0.25 pF	6.25 A	DFN1006LD-3	2	
	PESD5V0C1ULS-Q	5 V	0.6 pF	6.5 A	DFN1006BD-2	1	DFN package with SWF
	PESD5V0C1BLS-Q	5V	0.3 pF	6.5 A	DFN1006BD-2	1	DFN package with SWF
	PESD5V0C2UM-Q	5 V	0.5 pF	6.5 A	DFN1006-3	2	
	PESD4V0X2UM	4 V	0.82 pF	1.5 A	DFN1006-3	2	
	PESD15VW1UCSF	15 V	1 pF	18.5 A	DSN0603-2	1	
	IP3319CX6	5 V	1.5 pF (CMF)	7.5 A	WLCSP6	2 + 1 (ID)	
ID	PESD5V0S1BL-Q	5 V	152 pF	12 A	DFN1006-3	1	
	PESD5V0C1ULS-Q	5 V	0.6 pF	6.5 A	DFN1006BD-2	1	DFN package with SWF
	PESD5V0C1BLS-Q	5 V	0.3 pF	6.5 A	DFN1006BD-2	1	DFN package with SWF
	PESD5V0S1USF	5 V	35 pF	3.5 A	DSN0603-2	1	

USB3.2 Gen 1

Table 7: Product proposals for USB3.2 Gen 1

Signal name	Type name	V_{RWM}	C_d(typ)	I_{PPM} for t_P = 8/20 µs	Package name	Number of lines
RX, TX	PESD3V3Z1BCSF	3.3 V	0.45 pF	15 A	DSN0603-2	1
	PESD4V0W1BCSF	4.0 V	0.55 pF	20 A	DSN0603-2	1
	PESD5V5X1BCL-Q	5.0 V	0.49 pF	1.7 A	DFN1006-2	1
	PESD3V3C2UM	3.3 V	0.4 pF	6.5 A	DFN1006-3	2
	PESD4V0Z2BCDF	4 V	0.31 pF	11 A	DFN0603-3	2
	PUSB3FS4	3.3 V	0.29 pF	6.5 A	DFN2510A-10	4
	PUSB3FR6	3.3 V	0.35 pF	7 A	DFN2111-7	6
	PCMFxUSB3S	5 V	0.25 pF (CMF)	7 A	WLCSP5, 10, 15	2,4,6
	PESD5V0H1BLL-Q	5 V	0.25 pF	6.5 A	DFN1006L-2	1
	PESD5V0H1BLG-Q	5 V	0.25 pF	6.25 A	DFN1006LD-2	1
	PESD5V0H2BFG-Q	5 V	0.25 pF	6.25 A	DFN1006LD-3	2
	PESD5V0C1ULS-Q	5 V	0.6 pF	6.5 A	DFN1006BD-2	1
	PESD5V0C1BLS-Q	5 V	0.3 pF	6.5 A	DFN1006BD-2	1
CC/SBU	PESD24VV1BSF	24 V	9.3 pF	4.7 A	DSN0603-2	1
	PESD24VV1BL	24 V	14 pF	3.5 A	DFN1006-2	1
	PESD1IVN24LS-Q	24 V	14 pF	3.5 A	DFN1006BD-2	1
	PESD5V0X1BCAL	5 V	0.85 pF	1.8 A	DFN1006-2	1
	PESD5V0X2UAM(B)-Q	5 V	0.8 pF	2.5 A	DFN1006(B)-3	2

USB3.2 Gen 2

Table 8: Product proposals for USB3.2 Gen 2

Signal name	Type name	V_{RWM}	C_d(typ)	I_{PPM} for t_P = 8/20 µs	Package name	Number of lines
RX, TX	PESD4V0Z1BSF	4 V	0.24 pF	9.5 A	DSN0603-2	1
	PESD3V3C1BSF	3.3 V	0.2 pF	9 A	DSN0603-2	1
	PESD9V0C1BSF	9 V	0.2 pF	9 A	DSN0603-2	1
	PESD1V0Y1BIF	1 V	0.18 pF	6 A	DSN0603-2	1
	PUSB3BB4	3.3 V	0.17 pF	6.5 A	DFN2510A-10	4
	PESD5V0C2BDF	5 V	0.21 pF	8 A	DFN0603-3	2
	PUSB3FA2	1.65 V	0.17 pF	7 A	DFN2510A-10	4
	PESD5V0H1BLL-Q	5 V	0.25 pF	6.5 A	DFN1006L-2	1
	PESD5V0H1BLG-Q	5 V	0.25 pF	6.25 A	DFN1006LD-2	1
	PESD5V0H2BFG-Q	5 V	0.25 pF	6.25 A	DFN1006LD-3	2
	PESD5V0C1ULS-Q	5 V	0.6 pF	6.5 A	DFN1006BD-2	1
	PESD5V0C1BLS-Q	5 V	0.3 pF	6.5 A	DFN1006BD-2	1

USB 4 Gen 3

Table 9: Product proposals for USB4 Gen 4

Signal name	Type name	V_{RWM}	C_d(typ)	I_{PPM} for t_P = 8/20 µs	Package name	Number of lines
RX,TX	PESD1V0Y1BBSF	1 V	0.16 pF	5.5 A	DSN0603-2	1
	PESD4V0Y1BCSF	4 V	0.16 pF	5.5 A	DSN0603-2	1
	PESD18VY1BBIF	18 V	0.15 pF	tbd	DSN0603-2	1
	PESD5V0R1BDSF-Q	5 V	0.13 pF	4.8 A	DSN0603-2	1
	PESD5V0H1BLL(-Q)	5 V	0.25 pF	6.5 A	DFN1006L-2	1
	PESD5V0H1BLG-Q	5 V	0.25 pF	6.25 A	DFN1006LD-2	1
	PESD5V0H2BFG-Q	5 V	0.25 pF	6.25 A	DFN1006LD-3	2

HDMI Interfaces

Table 10: Product Proposals for HDMI interfaces

Signal name	Type name	V_{RWM}	C_d(typ)	I_{PPM} for t_P = 8/20 µs	Package name	Number of lines
TMDS/ FRL	PHDMI2AB4	5 V	0.17 pF	7 A	DFN2510A-10	4 (HDMI2)
	PHDMI2FR4	5 V	0.29 pF	7 A	DFN2510A-10	4 (HDMI1)
	PCMFxHDMI14S	5 V	0.25 pF	7 A	WLCSP5, 10, 15	2, 4, 6; (HDMI1)
	PCMFxHDMI2BA	4 V	0.3 pF	7.5 A	WLCSP5, 10, 15	2, 4, 6; (HDMI2)
	PESD3V3C1BSF	3.3 V	0.2 pF	9 A	DSN0603-2	1
	PESD5V0R1BDSF-Q	5	0.1	4.8 A	DSN0603-2	1
	PESD5V0H1BLL-Q	5 V	0.25 pF	6.5 A	DFN1006L-2	1
	PESD5V0H1BLG-Q	5 V	0.25 pF	6.25 A	DFN1006LD-2	1
	PESD5V0H2BFG-Q	5 V	0.25 pF	6.25 A	DFN1006LD-3	2
CEC	PESD5V0S1BL-Q	5 V	35 pF	12 A	DFN1006-2	1
DDC (I^2C)	PESD5V0V1BL-Q	5 V	11 pF	4.8 A	DFN1006-2	1
HEC	PESD5V0X1BCAL	5 V	0.85 pF	1.8 A	DFN1006-2	1
Hotplug	PTVS5V0Z1ULC	5 V	160 pF	44 A	DFN1006-2	1

LIN, CAN, CAN-FD and FlexRay interfaces, leaded packages

Table 11: Product Proposals for CAN, LIN and CAN-FD interfaces

Signal name	Type name	V_{RWM}	C_d(typ)	I_{PPM} for t_P = 8/20 µs	Package name	Number of lines
LIN, CANH, CANL	PESD2CANFD24U-X	24 V	3.2 pF	1.9 A	X = T, SOT23 X = U, SOT323	2
	PESD2CANFD24V-X	24 V	5.2 pF	2.6 A	X = T, SOT23 X = U, SOT323	2
	PESD2CANFD24L-X	24 V	9 pF	4 A	X = T, SOT23 X = U, SOT323	2
	PESD2CANFD27U-X	27 V	3.6 pF	1.8 A	X = T, SOT23 X = U, SOT323	2
	PESD2CANFD27V-X	27 V	5.2 pF	2.5 A	X = T, SOT23 X = U, SOT323	2
	PESD2CANFD27L-X	27 V	9 pF	3.9 A	X = T, SOT23 X = U, SOT323	2
	PESD2CANFD36UX-Q	36 V	4.3 pF	1.5 A	X = T, SOT23 X = U, SOT323	2
	PESD2CANFD36VX-Q	36 V	6 pF	2 A	X = T, SOT23 X = U, SOT323	2
	PESD2CANFD36LX-Q	36 V	10 pF	3.2 A	X = T, SOT23 X = U, SOT323	2
	PESD2CANFD54VT-Q	54 V	3.6 pF	2.8 A	SOT23	2
	PESD2CANFD54LT-Q	54 V	6 pF	4 A	SOT23	2
	PESD2CANFD60VT-Q	60 V	3.6 pF	2.6 A	SOT23	2
	PESD2CANFD60LT-Q	60 V	6 pF	4 A	SOT23	2
	PESD2CANFD72VT-Q	72 V	3.4 pF	1.9 A	SOT23	2
	PESD2CANFD72LT-Q	72 V	5.4 pF	3 A	SOT23	2

CAN and CAN-FD interfaces, leadless packages

Table 12: Product Proposals for CAN and CAN-FD interfaces with leadless packages

Signal name	Type name	V_{RWM}	C_d(typ)	I_{PPM} for t_P = 8/20 µs	Package name	Number of lines
CANH, CANL	PESD1CANFD24L(S)-Q	24 V	10 pF	3.8 A	SOD882(BD)	1
	PESD1CANFD30L(S)-Q	30V	9.8 pF	3.9 A	SOD882(BD)	1
	PESD1CANFD33L(S)-Q	33 V	9.8 pF	3.9 A	SOD882(BD)	1
	PESD1CANFD36L(S)-Q	36 V	8.7 pF	2.9 A	SOD882(BD)	1
	PESD2CANFD33UQB-Q	33 V	4.1 pF	2 A	DFN1110D-3	2
	PESD2CANFD36xQB(C)-Q	36 V	x = U, 3.9 pF x = V, 5.4 pF x = L, 8.7 pF	x = U, 1.6 A x = V, 2.3 A x = L, 2.9 A	B version = DFN1010D-3 C version = DFN1412D-3	2

CAN protection enhanced performance

Table 13: Product Proposals for CAN interfaces with enhanced performance in SOT23 packages

Signal name	Type name	V_{RWM}	C_d(typ)	I_{PPM} for t_P = 8/20 µs	Package name	Number of lines
CANH, CANL	PESD2CAN24T-Q	24 V	13.5 pF	5.3 A	SOT23	2
	PESD2CAN24LT-Q	24 V	25 pF	9 A	SOT23	2
	PESD2CAN24XLT-Q	24 V	31 pF	12 A	SOT23	2

Automotive Ethernet

The ESD protection devices listed below have a trigger voltage bigger than 100 V as recommended by the OPEN ALLIANCE.

Table 14: Product Proposals for Ethernet interfaces 10Base-T1S, 100Base-T1 and 1000Base-T1 with $V_{trigger}$ > 100 V

Type name	V_{RWM}	C_d(typ)	I_{PPM} for t_P = 8/20 µs	Package name	Number of lines
PESD2ETH100T-Q	24 V	2.5 pF	3.2 A	SOT23	2
PESD2ETH1GT-Q	24 V	1.8 pF	2.3 A	SOT23	2
PESD2ETH1GXT-Q	24 V	1.1 pF	2.3 A	SOT23	2
PESD1ETH1GLS-Q	24 V	1.5 pF	2.3 A	DFN1006BD-2	1
PESD1ETH1GXLS-Q	24 V	0.9 pF	2.3 A	DFN1006BD-2	1

The components shiwn in Table 15 suitable for 10Base-T1S, 100Base-T1 and 1000Base-T1 ethernet interfaces. They can be implemented for board-net voltages of 12 V, 24 V and 48 V.

Table 15: Product Proposals for Ethernet interfaces 10Base-T1S, 100Base-T1 and 1000Base-T1 with $V_{trigger}$ > 100 V

Type name	V_{RWM}	C_d(typ)	I_{PPM} for t_P = 8/20 µs	Package name	Number of lines
PESD1ETH10L-Q	75 V	0.35 pF	2.5 A	DFN1006-2	1
PESD1ETH10LS-Q	75 V	0.35 pF	2.5 A	DFN1006BD-2	1

For the ESD protection of an Ethernet interface the protection devices can be placed at the connector side but then require a V_{RWM} rating bigger than the battery voltage. The other option is to place them behind the coupling capacitors towards the I/O pins of the SoC used. Proposals of suitable products are listed in Table 17.

Table 16: Ethernet protection options at the connector (higher V_{RWM}) and at the SoC side (low V_{RWM} possible)

Placement Option	Type name	V_{RWM}	C_d(typ)	I_{PPM} for t_P = 8/20 µs	Package name	Number of lines
At the connector	PESD18VF1BL-Q	18 V	0.35 pF	1 A	DFN1006-2	1
	PESD24VF1BL-Q	24 V	0.3 pF	1 A	DFN1006-2	1
	PESD30VF1BL-Q	30 V	0.27 pF	1 A	DFN1006-2	1
	PESD18VF1BLS-Q	18 V	0.31 pF	–	DFN1006BD-2	1
	PESD24VF1BLS-Q	24 V	0.28 pF	–	DFN1006BD-2	1
	PESD32VF1BLS-Q	32 V	0.28 pF	–	DFN1006BD-2	1
	PESD18VF1BLG-Q	18 V	0.22 pF	–	DFN1006LD-2	1
	PESD24VF1BLG-Q	24 V	0.2 pF	–	DFN1006LD-2	1
	PESD30VF1BLG-Q	30 V	0.18 pF	–	DFN1006LD-2	1
Behind capacitors/at the PHY pins	PESD5V0F1BL-Q	5.5 V	0.4 pF	2.5 A	DFN1006-2	1
	PESD5V0F1BLD-Q	5.5 V	0.4 pF	2.5 A	DFN1006BD-2	1
	PESD4USB3(5)-TBR-Q	3.3/5 V	0.3 pF	–	DFN2510A-10	4
	PESD5V0C1BLS-Q	5 V	0.3 pF (max)	6.5 A	DFN1006BD-2	1
	PESD5V0H1BLL-Q	5 V	0.25 pF	6.5 A	DFN1006L-2	1
	PESD5V0H1BLG-Q	5 V	0.25 pF	6.25 A	DFN1006LD-2	1
	PESD5V0H2BFG-Q	5 V	0.25 pF	6.25 A	DFN1006LD-3	2

High-Speed Video Links, SerDes

Table 17: High-speed Video Links and SerDes protection options at the connector (higher V_{RWM}) and at the SoC side (low V_{RWM} possible)

Placement Option	Type name	V_{RWM}	C_d(typ)	I_{PPM} for t_P = 8/20 µs	Package name	Number of lines
At the connector	PESD18VF1BL-Q	18 V	0.35 pF	1 A	DFN1006-2	1
	PESD18VF1BLS-Q	18 V	0.31 pF	–	DFN1006BD-2	1
	PESD24VF1BL-Q	24 V	0.3 pF	1 A	DFN1006-2	1
	PESD24VF1BLS-Q	24 V	0.28 pF	–	DFN1006BD-2	1
	PESD30VF1BL-Q	30 V	0.28 pF	1 A	DFN1006-2	1
	PESD30VF1BLS-Q	30 V	0.28 pF	–	DFN1006BD-2	1
	PESD18VF1BLG-Q	18 V	0.22 pF	–	DFN1006LD-2	1
	PESD24VF1BLG-Q	24 V	0.2 pF	–	DFN1006LD-2	1
	PESD30VF1BLG-Q	30 V	0.18 pF	–	DFN1006LD-2	1
Behind capacitors/at the PHY pins	PESD5V0F1BL-Q	5.5 V	0.4 pF	2.5 A	DFN1006-2	1
	PESD5V0F1BLD-Q	5.5 V	0.4 pF	2.5 A	DFN1006BD-2	1
	PESD5V0C1BLS-Q	5 V	0.3 pF (max)	6.5 A	DFN1006BD-2	1
	PESD5V0C1ULS-Q	5 V	0.6 pF (max)	6.5 A	DFN1006BD-2	1
	PESD5V0C2UM	5 V	0.5 pF	6.5 A	DFN1006-3	2
	PESD5V0H1BLL-Q	5 V	0.25 pF	6.5 A	DFN1006L-2	1
	PESD5V0H1BLG-Q	5 V	0.25 pF	6.25 A	DFN1006LD-2	1
	PESD5V0H2BFG-Q	5 V	0.25 pF	6.25 A	DFN1006LD-3	2
	PESD4USB3/5B-TBS	3.3 V/ 5 V	0.24 pF	7 A	DFN2510D	4
	PESD4USB3/5U-TBS	3.3 V/ 5 V	0.4 pF	7 A	DFN2510D	4

15.3 TVS-Diodes, Power supply protection

Nexperia calls protection diodes with a very high surge rating, large die sizes and a comparably high diode capacitance Cd TVS diodes. The main application area for such diodes are supply voltages.

Table 1: Product proposals TVS-Diodes

Type name	V_{RWM}	10/1000µs surge rating	I_{PPM} for t_P = 8/20 µs	Package name	Number of lines	Comments
PTVSxxVS1U(T)R-(Q) series	3.3 V – 64 V	400 W	–	CFP-3	1	Tj(max) = 185°C for T-version, uni-directional
PTVSxxVP1U(T)P-(Q) series	3.3 V – 64 V	600 W	–	CFP-5	1	Tj(max) = 185°C for T-version unidirectional
PTVSxxVP1BPL	9 V – 160 V	600W	–	CFP-5-FL	1	bidirectional
PTVSxxZ1USK	5 V – 26 V	200 W	80A (5 V) 32A (26 V)	DSN1608-2	1	unidirectional
PTVS5VZ1USKN	5 V	260 W	100 A	DSN1608-2	1	unidirectional
PTVSxxZ1BSC	3.3V, 5 V	-	70A, 60 A	DSN1006-2	1	unidirectional
PTVSxxZ1UPC	4.8 V, 5 V, 5.5 V and 6.3 V		150 A, 150 A, 140 A & 140 A	DFN1610-2	1	unidirectional
PTVSxxU1UPA	7.5 V – 26 V		178 A (7.5 V) – 69 A (26 V)	DFN2020-3	1	unidirectional
PTVSxxZ1UPA	24 V, 30 V		150 A	DFN2020-3		unidirectional

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